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Final Report of the Silicon Lifetime Committee

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Abstract

The Silicon Lifetime Committee was charged with systematically identifying limitations to the operational lifetime of the present silicon detectors, SVX II, ISL, and L00. In this note the work and conclusions of this committee are summarized.

Contents

1 Introduction

In the summer of 2003 the Run IIB silicon detector upgrades were canceled. This implied that the Run IIA detectors had to last the whole of Run II, presently scheduled to run through Oct-2009. Not all the Run IIA detectors (SVX II, ISL, L00) were designed to last that long. In particular SVX II and L00 were designed to last for approximately 2 fb^{-1} and 4 fb^{-1}, respectively. The cancellation of the Run IIB upgrades effectively required a doubling or tripling the operational lifetime of these detectors. The Silicon Lifetime Committee (SLC) was formed to systematically consider what needs to be done to help meet this challenge. The committee acknowledges the work done by the Silicon Run IIB committee [1], some of which we use directly as noted below.

1.1 Committee Membership and Charge

The committee charge was:

1. Systematically identify all possible sources of silicon detector inefficiency.

2. Identify means of mitigating these inefficiencies and/or, where necessary, make suggestions for better quantifying/understanding long term projections of detector performance.

3. Develop a (prioritized) list of action items to help maximize the detector efficiency for the duration of Run II.

For these purposes we defined "perfect success" as maintaining the present level of performance through Run II, and did not specifically consider means of recovering ladders which are presently unable to take data. Such involved "rescue" efforts were deemed to be beyond the scope of this committee. We discuss the present state of the detector and some of the causes of permanent damage later, in section 2.

The committee membership was N. Bacchetta, G. Bolla, D. Glenzinski (chair), P. Lukens, V. Pavlicek, J. Spalding, R. Stanek, W. Trischuk, and R. Wallny. In addition, it took input from many people within the silicon operations [2] and radiation monitoring [3] groups and solicited specific advice from some people outside CDF as well.

The committee met about twice a month from February-2004 to June-2004. Meeting minutes and other documentation are available at `http://www-cdf.fnal.gov/internal/silicon/longevity/longevity.html`.

1.2 Committee Work Plan

The committee organized itself in the following manner. It separately considered the damage history for the SVX II, ISL, and L00 - and was particularly concerned with identifying sources of permanent damage which were either not fully understood or were growing. The committee also took a systematic look at other effects which might limit the lifetime of the detectors. These studies were broadly classified into three categories: the Inevitable, the

Preventable, and the Miscellaneous. An "Inevitable" effect is anything which detrimentally affects the performance of the detector, but which is an inherent part of detector operation (*e.g.* radiation damage). A "Preventable" effect is anything which *would* detrimentally affect the performance of the detector *if* appropriate steps are not taken (*e.g.* an inadequate pool of working spares). Any effect which did not readily fall into one of these categories was classified as a "Miscellaneous" effect. The principal use of defining the categories was to help organize the committee's efforts and should not be interpreted too stringently. Indeed, there are a few effects which could easily have been classified in more than one of the categories. They are discussed here in the category in which we first happened to consider them.

In the next section the damage histories are discussed. Then we summarize our findings for each of the three categories. We have a section which discusses other possible upgrade scenarios. Finally, we give a prioritized list of action items and then conclude. Much of the detail is presented in the Appendices.

2 Damage Histories

Over the last few years the silicon operations sub-project leaders (SPL) have been keeping close track of chip failures in the silicon detectors. Figure 1 shows the fraction of each detector that has been integrated into data-taking as a function of time beginning in Jan-2002. After the commissioning ramp-up approximately 92%, 85% and 95% of the SVX II, ISL and L00, respectively, have been steadily taking data. Each failure is categorized as it becomes understood. It is important to keep track of failure trends in order to spot those categories which continue to grow. In Figures 2 to 4 the damage histories for the SVX II and ISL are shown. In each figure, the fraction of chips which are inoperable (*i.e.* unable to take (good) data) is plotted as a function of time. The various sources of damage are broken-out into separate curves. We briefly discuss these figures below.

2.1 SVX II History

The SVX II damage history is shown in Figures 2 and 3 for the phi and z-sides, respectively. There are two major sources of damage, trigger resonances (which usually affect the DVDD lines) and AVDD2 failures. The trigger resonances are now prevented by a combination of operational guidelines and the Resonance GhostBuster Board, which halts a run when a resonance condition is detected. Since the implementation of the operational guidelines in late-2002 there have been no more chips lost due to trigger resonances. With the introduction of the Resonance GhostBuster the SVX II is able to cope with level 1 trigger rates in excess of 20 kHz (the present operational limit is 30 kHz, but may be increased as experience is gained at these higher rates). The AVDD2 problems have been accumulating since the commissioning phase. A summary of some early investigations can be found in cdfnote [4]. Most all the AVDD2 problems can be associated with either a beam accident in which CDF received a significant dose of radiation, or with a thermal cycle - usually related to an access. Although some considerable effort has been made, the exact mechanism for the AVDD2 failure is not understood. It is the only failure mechanism which continues to grow for the SVX II. Since

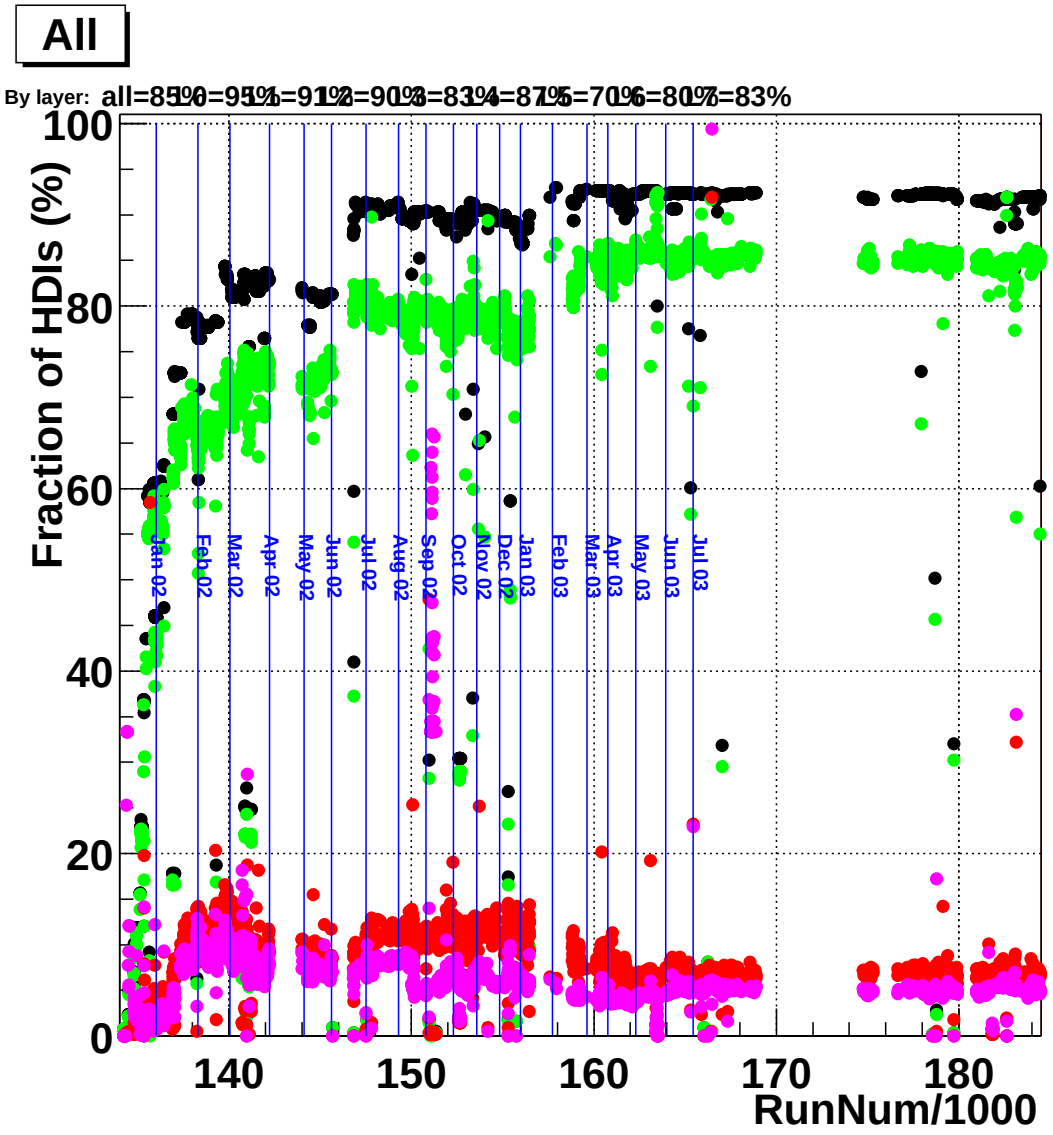

Figure 1: Fraction of HDIs integrated into data-taking as a function of run number. The black dots indicate the fraction of HDIs integrated into data-taking, while the green dots indicated that fraction of HDIs integrated into data-taking which yield $< 1\%$ readout errors. The red and pink dots keep track of bad ladders and error rates, respectively.

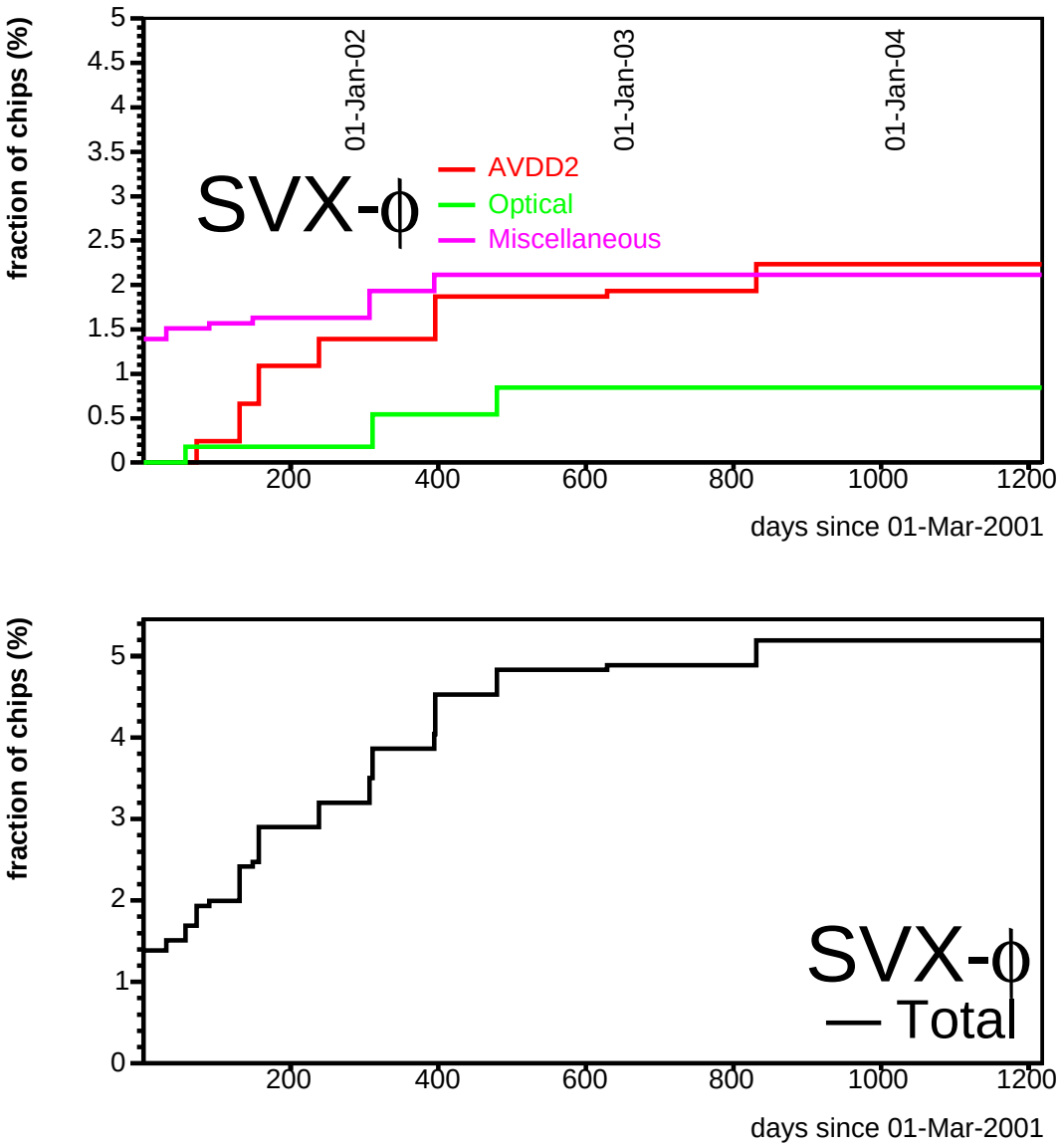

Figure 2: Damage history of the SVX-ϕ side, expressed as the fraction of readout chips which are inoperable. The AVDD2 failures are mostly due to beam incidents and/or thermal cycles. The last optical failure (at $x \approx 500$) was due to a trigger resonance.

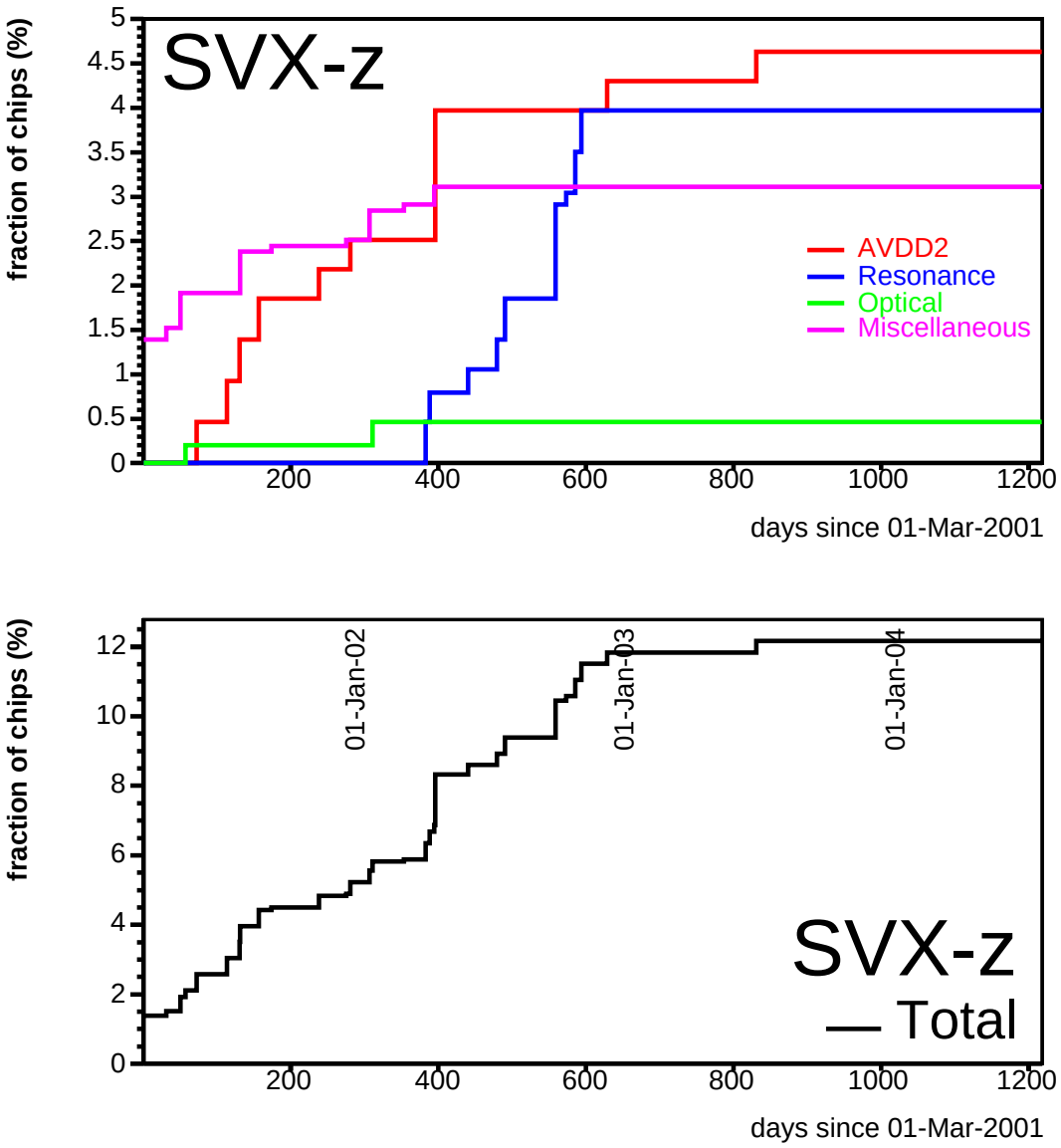

Figure 3: Damage history of the SVX-z side, expressed as the fraction of readout chips which are inoperable. The AVDD2 failures are mostly due to beam incidents and/or thermal cycles.

recovery of these chips seems very unlikely, we will concentrate instead on possible means of mitigating these failures.

2.2 ISL History

The ISL damage history is shown in Figure 4. There are two major sources of lost data, the cooling blockage and "Front-End Oscillations" (FE-Oscillations). Although most of the blocked cooling lines were recovered, 1 blocked line remains. There is little chance that it will ever be opened. A concerted effort may be able to determine operating parameters which would allow at least a partial recovery of the affected 10 ladders. The FE-Oscillation failures, like the AVDD2 failures, are most always associated with beam accidents. No concerted investigation has been made to understand these failures. They are the major source of continuing ISL failures.

2.3 L00 History

For L00, less than 5% of the chips are permanently damaged. Of those, most were known since installation. The remaining losses are due to a variety of causes. While at present there is no single contributing source of L00 damage, it should continue to be monitored with the same diligence accorded to the SVX II and ISL systems.

2.4 Portcard and Junction Card History

Throughout all 3 silicon systems 2 portcards and 1 junction card have failed (there are 114 of each employed in B0). One of the portcard failures was present since installation and is assumed to have been damaged during transport from SiDet to CDF. The other portcard failure occurred spontaneously and is not fully understood. The junction card failure is also not understood. Fortunately the failure occurred in an accessible part of the card and could be repaired.

Both portcard and junction card failures can affect a full wedge, and must be monitored very closely. Depending on the location of the failure, the junction cards can be repaired *in situ*. The portcards, on the other hand, are inaccessible. Any evidence that such failures are happening with some regularity needs to be taken very seriously and concerted investigations to understand and mitigate the underlying causes should be undertaken immediately.

3 The Inevitable Effects

The committee identified only one Inevitable Effect which may limit the lifetime of the detector - radiation damage. The detector response to radiation dose has been well documented, most recently in reference [5]. Assuming 8 fb^{-1} of delivered luminosity by the end of FY09, the signal-to-noise ratio on all layers, both phi and stereo sides, should remain ≥ 8, except for L00, where it is expected to be about 6. These S/N ratios should not cause any serious problems in terms of readout occupancy, pattern recognition, SVT performance or B-tagging. A possibly

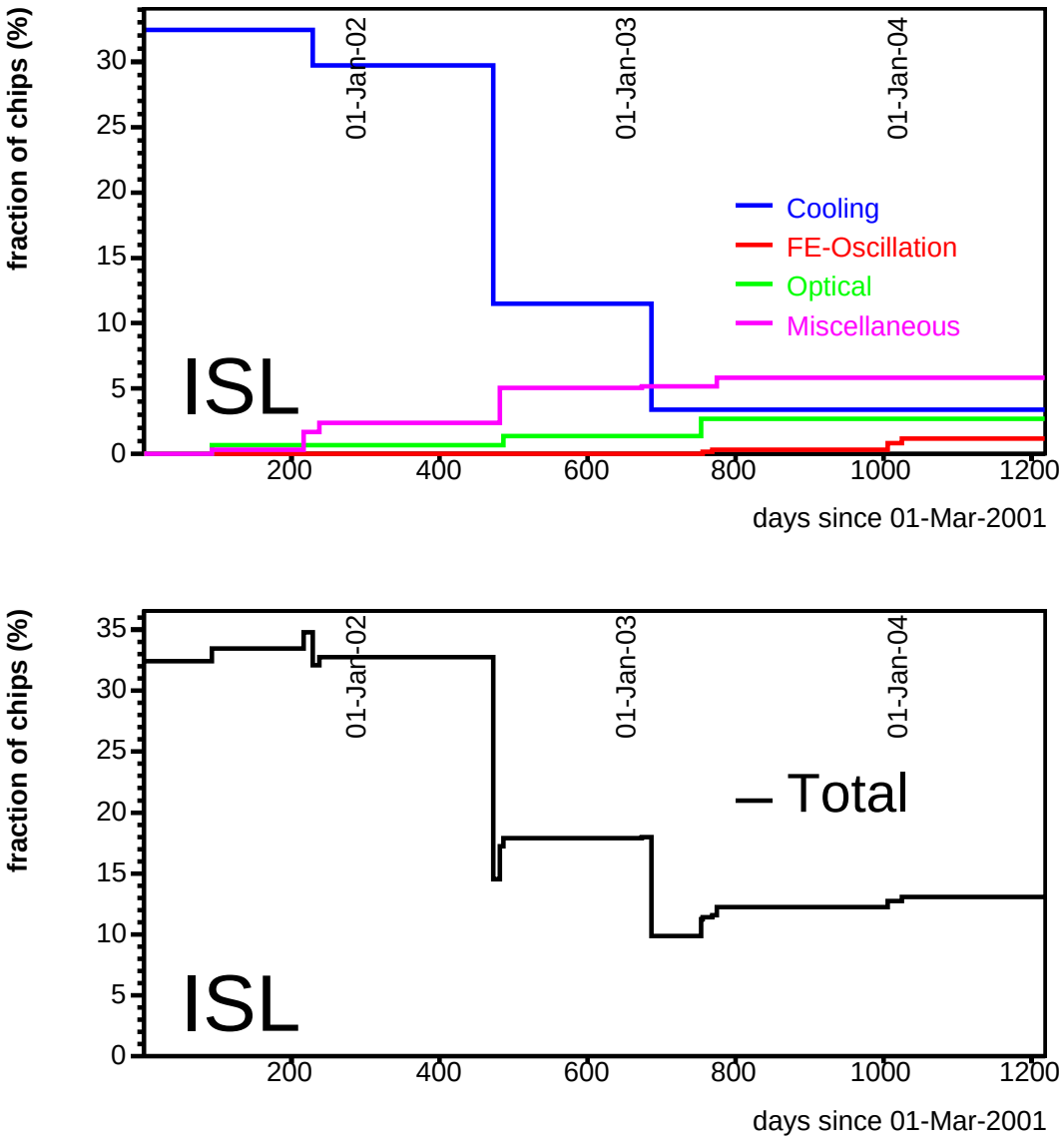

Figure 4: Damage history of ISL (ϕ and z), expressed as the fraction of chips which are inoperable. The cooling failures are due to the epoxy blockages. The FE-Oscillations may be beam related.

more serious limitation comes from the required bias voltages necessary to deplete the bulk silicon for efficient charge collection. The readout capacitors on all the SVX II and ISL sensors are rated to about 100 volts and were burned-in at 90 volts. Applying voltages above that can cause capacitive breakdown, which compromises the chip performance. There are large uncertainties associated with projections of the necessary bias voltage, V_{bias}, as described in [5]. Using the central values, we expect the inner two layers of the SVX II to require bias voltages in excess of 180 volts ($\pm$90 volts on each side) after approximately 7 fb^{-1}. This luminosity cutoff can vary between $6 - 9$ fb^{-1} when choosing the parameters of the damage model differently. Note that this is a limitation of the sensors, and cannot be mitigated with upgrades to the power supplies, which were designed to deliver up to 5 mA at 250 volts ($\pm$125 volts on each side).

The principal means of mitigating the effects of radiation damage is by running colder. Lowering the operating temperature of the SVX II an additional $4^{\circ}C$ (to $-10^{\circ}C$) is expected to extend the lifetime of the inner layers by an additional 1 fb^{-1}. This should be readily achievable since the detector (SVX II + L00) and the cooling system were designed and built to run at $-10^{\circ}C$. It is too early to tell if running even colder is warranted and will depend on how the depletion voltages change with increased radiation damage. At present, the depletion voltages are changing at a rate that's very close to what was assumed in the extrapolations above. Limiting the number of times the silicon is warmed to room temperature can also help mitigate the effects of radiation damage, although to a more limited extent than running colder.

The committee suggests that the work to run the silicon colder begin immediately. Given the uncertainties in extrapolating the effects of large radiation doses, the committee also recommends that the monitoring of detector performance (*e.g.* depletion voltages) be more thorough, better coordinated, and more frequently updated. Particular attention should be paid to any unexpected behavior which might suggest a more rapid performance degradation and/or an additional source of performance degradation. The present monitoring effort is not as robust, thorough, or formal as it ought to be. The committee also suggests completing the installation of the "silicon baggy", which will reduce the number of times the silicon must be brought to room temperature, as soon as possible. Although these thermal cycles may have only a small effect on radiation damage induced inefficiencies, they are suspected of playing a much larger role in causing AVDD2 failures in the SVX II.

4 The Preventable Effects

To assess the "Preventable" sources of performance degradation, the committee divided the silicon system into sub-systems and performed a vulnerability study on each. The sub-systems were: DAQ, SRC, Resonance GhostBuster, cables, power supplies, junction cards, cooling, interlocks, and radiation safety. The vulnerability studies are included in the appendices. We summarize them here.

For each sub-system, in consultation with the relevant experts, we tried to address the following set of questions:

- Do specs change now that FY09 is the expected lifetime
  - due to increased radiation dose?
  - due to performance "expectations" from other Run IIB upgrades?
  - due to changing accelerator conditions?
- Will the performance meet the (new) specs in FY09?
- Is there some way to help ensure or improve chances of successfully meeting specs in FY09 or is significant improvement possible?
- Is there a persistent failure mode that's not understood?
- Is the spare pool sufficient, maintained, and will it last to FY10 (*e.g.* if spare pool is shrinking with time, does it extrapolate to FY10?)?
- Are the test facilities sufficient and maintained?
- Will expertise be available and/or are the system and its procedures thoroughly documented?

Questions were added or removed as appropriate for the sub-system in question. Although the specific suggestions vary from sub-system to sub-system, we can identify two principal concerns which affect most of these sub-systems.

Overall, we found the sub-systems, as a whole, to be in pretty good shape. All are expected to meet their performance specifications through the whole of Run II and most have a sufficient spare pool and well maintained test facilities. The most worrisome shortcoming, across all sub-systems, is the degradation and/or loss of expertise. Our recommendations are detailed for each sub-system in the Appendices, but we highlight some important conclusions from these studies in the next paragraphs.

First and foremost, the optimal performance of nearly every sub-system is threatened by a loss or degradation of resident expertise or inadequate effort. This is probably the most serious challenge facing the silicon operations group. It is extremely important for CDF institutions to fulfill their MOU responsibilities. Moreover, a concerted effort needs to be made with the silicon group to thoroughly document the salient features and procedures for each sub-system. The most worrying inadequacies are for the SRC, the Resonance GhostBuster, and the Siemens interlock ladder-logic. These need to be addressed immediately before the present generation of experts leaves CDF.

Second, many sub-systems have service contracts or MOUs- either with vendors, with technical support groups at FNAL, or with university groups- which need to be formally extended. This should happen immediately. Similarly, many sub-systems need to keep their test stands operational for longer than originally guessed - appropriate arrangements need to be made so that those test stands are maintained and that access to them continues through Run II.

As possible single-point-failures in the silicon system, the committee was particularly concerned with the SRC and the interlocks. While both systems have so far run very reliably, it

seems prudent to ensure a set of hot spares are available. This is especially true since some of the hardware used in these systems is becoming (or is already) obsolete - so that spare parts may be difficult to obtain. The committee would like to see an immediate effort to commission a full set of hot spares for both of these systems. The specific recommendations are in the appendices.

5 The Miscellaneous Effects

The committee considered only one Miscellaneous Effect - damage or inefficiencies caused by beam interactions. We include both beam-accident induced damage and beam-halo induced single-event-upsets.

It should be noted that there have been several beam accidents which have resulted in permanent detector damage. In many of these instances the risk to the CDF silicon has been mitigated after a thorough study of the accident. The committee tried to assess whether or not we ought be more pro-active about identifying these mitigations. Any such work would have to occur in close collaboration with the Accelerator Division. Some specific suggestions are discussed in Appendix I in the subsection labeled, "Fast Beam Accidents". In particular it is recommended to optimally position the A11 and A48 collimators using dedicated studies and to work with AD to formalize procedures which improve the robustness of the abort kickers and to reduce the number of kicker pre-fires.

There are also occasional and spurious failures of some silicon power supplies and DAQ boards in the collision hall. These presently occur at a fairly low rate and are not considered to be a significant contributor to detector downtime. However, their cause is not thoroughly understood. There is anecdotal evidence that these failures may be beam-halo induced single-event upsets occurring in specific components of the affected boards. The CDF radiation monitoring group has a very thorough set of measurements which characterize the radiation environment in the collision hall. The committee recommends that the silicon operations group work closely with the radiation monitoring group to try and establish a firm correlation between these failures and beam-halo activity in the collision hall. The frequency of these failures should also be monitored as they might be expected to significantly increase as the Tevatron luminosity continues to improve.

6 Upgrade Possibilities

With the cancellation of the full Run IIB upgrades, several partial upgrades were further considered. We discuss each of these briefly below.

6.1 Replace L00

A replacement of L00 which includes mitigations for the noise pick-up might more readily be included into the SVT (and thereby mute the effect of decreased S/N - due to radiation damage - in the inner layers of SVX II). However, as detailed in cdfnote [6], such a replacement

entails *extreme* schedule and technical risk. Even ignoring those risks, it was not clear that the noise pick-up could be entirely mitigated (due to various existing constraints), nor that the detector could be aligned well enough to be included in the SVT. It was concluded that replacing L00 is not worth the associated risks.

6.2 Replace SRC

With the new Run IIB detector came a new DAQ. Most of that DAQ upgrade is unnecessary with the cancellation of the detector upgrade. However, there has been an ongoing discussion as to whether or not an upgrade to the SRC might still be beneficial. The status of the present SRC and the pros and cons of a replacement are discussed in the Appendix B. We summarize the discussion here.

The present SRC has performed very robustly, with no known failures since installation. There are 2 SRC boards used at B0 to take data, with an additional 6 boards available as potential spares. Not all of these 6 extra boards have the full set of ECOs implemented nor do they all have the latest firmware installed. The updating of these 6 boards is of extreme importance and should be accomplished as soon as possible. The committee also recognized that firmware changes to the SRC are dangerous to the detector (*e.g.* a bad sequence can put the chips in a high current state, potentially causing permanent damage). The procedure for testing and verifying a firmware change, prior to its introduction into the B0 boards, should be documented and formalized as a "Systems Change Request" with the CDF Operations Department. Additional suggestions to strengthen the maintainability of the present system are given in the SRC Vulnerability Study in Appendix B. The implementation of these suggestions should make it unlikely that the SRC will limit the operational lifetime of the silicon system and should reduce the chances of incurring detector damage due to errant firmware changes. The committee thinks these recommendations should be pursued with high priority.

Although the committee concluded that the present SRC does not pose any significant risk to the detector itself, the committee is concerned that it may limit the trigger capabilities of the experiment as the luminosity increases. Some of the FPGAs on the present SRC with the present firmware use a majority of their capacity ($> 70 - 75\%$). This limits the flexibility of the present SRC to accommodate any future firmware changes which may be needed to handle an increase in trigger rate, trigger sophistication, or both. Dedicated studies have demonstrated that the present SRC with the present firmware can accommodate L1 trigger rates up to the Run IIA design specification of 50 kHz [7]. A systematic study of the specific causes of this rate limitation has not yet been completed. As such, it is difficult to conclude that a faster or more clever SRC would definitively and significantly improve the L1 trigger rate. Given this, the committee finds no compelling reason to advocate replacing the SRC. This conclusion could change as the ongoing studies mature. The principal advantage of a new board would be the increased flexibility it would have to accommodate changing trigger conditions. The principal risk is to the detector, since an SRC can cause permanent damage to the chips.

6.3 Replace Siemens PLC

With the new Run IIB detector also came a new Interlock system. In particular the Siemens PLC was to be replaced with a QuadLog/APACS PLC. The principal advantage of this replacement is that a large FNAL-resident pool of QuadLog/APACS expertise exists. In contrast, the Siemens expertise is concentrated in a few (mostly 1) university post-doc who could leave CDF. The principal disadvantage of the replacement is that it requires significant rewiring of the present inputs (to a QuadLog compatible I/O interface), and a re-write of the (non-trivial) interlock code - both of which will incur some downtime and risk permanent detector damage.

The present interlock system has been very robust since its installation in 2000 at CDF. Since that time there has been only one documented failure (a readout board). The software programs have been stable since 2001. The committee concludes that there is no compelling reason to upgrade the Siemens PLC. The interlock system is unlikely to limit the operational lifetime of the silicon system or to cause permanent detector damage. A more detailed list of recommendations can be found in Appendix H.

It should be mentioned that it may be possible to interface the Siemens I/O modules with a QuadLog PLC, thus eliminating the need to rewire the inputs and significantly reducing both the downtime and associated detector risk to upgrading the Siemens PLC to a QuadLog PLC. If this proves to be the case, the committee thinks the decision about whether or not to go ahead with the upgrade is best made by the Head of CDF Operations (presently Rob Roser) in consultation with the Silicon SPLs (presently Rainer Wallny and William Trischuk). A "Process Systems Change Procedure" for the interlock logic already exists as does the original Interlock ORC Procedure. These documents could serve to help develop a testing and check-out procedure which would minimize the detector risk.

6.4 Other Possibilities

Should it prove necessary to run the SVX chiller colder than $-10^{\circ}C$, some upgrade to the present cooling system may be required. However, tests performed for the Run IIB detector upgrade indicated that the chiller itself was capable of running stably at temperatures as cold as $-17^{\circ}C$ at about 20 lpm with a 6 kW heat load. The SVX II + L00 (both are cooled by the same chiller) generate about 2 kW of heat (total) and require a flow rate of about 20 lpm to keep temperature rises within design specifications. Thus, it seems likely that the chiller (the most expensive potential upgrade) would not need to be upgraded in order to run colder, although some other (minor) parts may need to be. The committee concluded that these small upgrades could readily be accommodated within the Operations budget should they prove necessary. The Head of the CDF Operations Department agreed with this conclusion. It should be noted that prior to making such a change, dedicated studies to determine the effect on the SVX II and L00 detectors would need to be performed. Since these detectors were built to run only to $-10^{\circ}C$, it may be they are unable to accommodate colder temperatures.

The committee identified no additional upgrade possibilities.

7 Conclusion

We have systematically considered effects which might limit the operational lifetime of the Run IIA silicon detectors, SVX II, ISL, and L00, and have made a list of recommendations to help mitigate these effects. A detailed set of specific suggestions is listed for each sub-system in the appendices. We summarize the recommendations here, in descending order of priority.

• Immediate Priority

Run Colder: The operating temperature of the SVX II + L00 should be lowered to $-10°C$ (for which they were originally designed) to help mitigate the effects of radiation damage. The sooner this happens, the more beneficial it is. The depletion voltages should be regularly monitored - an accelerated rate of change (relative to the collected luminosity) might warrant running even colder. The decision to run colder would need to proceed with extreme caution since the SVX II and L00 detectors were not designed to run colder than that. Dedicated detector and system studies would be required and a partial upgrade to the cooling system might also be necessary (*e.g.* new valves or fittings).

Install Si-Baggy: The silicon gas volume should be separated from the COT gas volume to help mitigate the effects of annealing, and to reduce the number of thermal cycles. The sooner this happens, the more beneficial it is.

Address SRC Concerns: A set of spare SRC boards should be tested. The status of all the SRC boards should be logged. The firmware should be documented. The firmware change procedure should be formalized with the CDF Operations Department in the same manner as the interlock change procedure.

Address Interlock Concerns: A test crate should be made operational. A spare PLC should be tested and made available. The ladder logic should be documented.

Update Maintenance Agreements: In addition to all the CDF MOUs, the following service contracts should be formally extended to the end of FY09: AD for the RadMon readout, PREP for the CAEN repairs, ESE for the DAQ boards and test stands, Yale for SRC burn-in, and UChicago for GhostBuster burn-in and testing.

Initiate AVDD2 and FEO Investigations: Dedicated efforts to understand the cause of "AVDD2" and "Front-End Oscillation" failures should be commissioned.

• Medium Term Priority

Recruit New Expertise: The participating CDF groups should provide the next generation of expertise as soon as possible so that they have an opportunity to overlap with the present set of experts. The reduction/dilution of expertise may be the most serious challenge facing the silicon operations group. The new round of MOUs is an ideal opportunity to address this worry and to incorporate the expertise of new groups.

Document Existing Expertise: All sub-systems should have their hardware, software, and relevant procedures thoroughly documented. At present, there is a wide disparity among the sub-systems - some are very thoroughly documented, others are very sparsely documented. The lack of documentation can be dangerous as expertise moves-on.

Improve Detector Monitoring: The Silicon Monitoring Group should be strengthened so that it more regularly and more thoroughly monitors the detector performance (*e.g.* ladder-by-ladder efficiency and resolution and related indicators). This is important not only to track the progress of radiation damage, but also to spot any abnormal or unexpected performance trend which might detrimentally affect the physics output of the detectors. This is particularly important since the decision about whether running colder is warranted will be based on the information collected and digested in this group.

Improve DOIM Monitoring: It may happen that, due to radiation damage, the output of the DOIM TX may move out of the RX response range for individual bits [8]. If this happens, whole ladder's worth of data may be lost - depending on which bit is affected. While the DOIMS are expected to survive the whole of Run II, it is important to monitor the DOIM response to increased radiation dose so that an abnormal or accelerated aging could be spotted early enough to develop a mitigation plan. For example, it may be possible to develop attenuators which could be used on single fibers at the input to the RX. In that case the DOIM voltages at the power supply could be adjusted to bring the lowest lying fibers back into range and the attenuators could be used to bring the highest lying fibers back into range.

Improve Collision Hall Monitoring: There is a class of power supply and DAQ board failures which may be caused by single-event-upsets induced by beam losses. In collaboration with the radiation monitoring group, an effort should be made to establish the correlation of these failures with beam losses. If the correlation is firmly established, appropriate mitigations should be developed and employed since the rate of such failures would then likely increase with increasing luminosity.

- ## Long Term Priority

Implement Vulnerability Recommendations: The remaining miscellaneous recommendations of the vulnerability studies ought to be implemented as detailed in the appendices.

References

[1] A. Affolder *et al.*, *Run IIB Silicon Working Group Report*, cdfnote 5425.

[2] The Silicon Operations Group web page is `http://www-cdf.fnal.gov/internal/silicon/scc.html`

[3] The Radiation Monitoring Group web page is `http://ncdf67/~tesarek/radiation`

[4] A. Affolder *et al.*, *Internal Failures of SVX II Ladders*, cdfnote 5817.

[5] S. Worm, *Life Expectancy of the Run II Silicon*, cfdnote 6773.

[6] G. Derylo, *Mechanical Feasibility of Layer00 Replacement in the CDF Collision Hall*, cdfnote 6943.

[7] Steve Nahn, personal communication.

[8] S. Hou and R.S. Lu, *DOIM Parallel Optical Links: TX/RX*, available at `http://www-cdf.fnal.gov/internal/silicon/longevity/docs/suen_031219.pdf`; M. Bishai *et al.*, *Dense Optical Interface Module for the CDF Run II Silicon Tracking System*, cfdnote 6497.

A DAQ Vulnerability Study

Summary: A review of the vulnerabilities of CDF silicon DAQ components.
Vince Pavlicek, May-2004

The specific modules are the fiber optic components connecting the detector to the DAQ and the DAQ VME modules.

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Glossary:

DOIM Dense Optical Interface Module - Fiber optic ribbon data link, 9 bits wide.

FIB Fiber Interface Board - reformattor and pre-processor for data from DOIMS

FFO FIB Fan-out - distributes clocks and commands for a FIB rack.

FTM FIB Transition Module - has the fiber receivers & resynchronizes the data.

VFO VRB Fan-out - distributes clocks and commands for a VRB rack.

VRB VME readout buffer - L2 data storage.

VTM VRB Transition Module - has the Glink receivers & resynchronizes the data.

* ---

Module: VRB Quantity available: 65. Quantity required 59.

Understand if specifications change now that 2010 is the expected lifetime due to increased radiation dose: n/a

Understand if specifications change due to performance expectations from other run2b upgrades: No, and there are unused readout modes.

Understand if specifications change due to changing accelerator conditions(3): There are rate effects, Steve, Mark

Understand if performance will meet the (new) specs in 2010:

```
  Yes, except size limit in buffers.

Is there some way to help ensure or improve chances of successfully meeting
  specs in 2010 or whether significant improvement is possible:
  Document firmware.

Ask if there's a persistent failure mode that's not understood:
  no, low firmware error rate.

Determine that spare pool is sufficient, maintained, and will last to 2010:
  yes (7)

Determine that test facilities are sufficient and maintained(4):
  yes, at PREP.

Determine that expertise will be available and/or that system and procedures
  are documented: yes.
Software Documentation? Good.
Hardware Documentation? Good.

* ------------------------------------------------------------------------

Module: FIB. Quantity available: 65.  Quantity required 58.

Understand if specifications change now that 2010 is the expected lifetime
  due to increased radiation dose: SEU increase but not tracked (1).

Understand if specifications change due to performance expectations from
  other run2b upgrades: No.

Understand if specifications change due to changing accelerator conditions(3):
  There are rate effects, Steve, Ken.

Understand if performance will meet the (new) specs in 2010:
  Yes, No expected limits.

Is there some way to help ensure or improve chances of successfully meeting
  specs in 2010 or whether significant improvement is possible:
  Document firmware.

Ask if there's a persistent failure mode that's not understood:
  no, low firmware error rate.
```

Determine that spare pool is sufficient, maintained, and will last to 2010:
  yes (7).

Determine that test facilities are sufficient and maintained(4):
  yes, at PREP.

Determine that expertise will be available and/or that system and procedures
  are documented: yes.
Software Documentation? No (2).
Hardware Documentation? Needs update.

* --

Module: VFO Quantity available: 9. Quantity required 7.

Understand if specifications change now that 2010 is the expected lifetime
  due to increased radiation dose: n/a

Understand if specifications change due to performance expectations from
  other run2b upgrades: No.

Understand if specifications change due to changing accelerator conditions(3):
  No.

Understand if performance will meet the (new) specs in 2010:
  Yes.

Is there some way to help ensure or improve chances of successfully meeting
  specs in 2010 or whether significant improvement is possible: No.

Ask if there's a persistent failure mode that's not understood:
  no.

Determine that spare pool is sufficient, maintained, and will last to 2010:
  yes (7).

Determine that test facilities are sufficient and maintained(4):
  yes, at PREP.

Determine that expertise will be available and/or that system and procedures
  are documented: yes.
Software Documentation? Good.
Hardware Documentation? Good.

```
* ------------------------------------------------------------------------

Module: FFO Quantity available: 14.  Quantity required 7.

Understand if specifications change now that 2010 is the expected lifetime
  due to increased radiation dose: No noticable SEU rate.

Understand if specifications change due to performance expectations from
  other run2b upgrades: No.

Understand if specifications change due to changing accelerator conditions(3):
  No rate effects, Steve, Stefano.

Understand if performance will meet the (new) specs in 2010:
  Yes.

Is there some way to help ensure or improve chances of successfully meeting
  specs in 2010 or whether significant improvement is possible: No.

Ask if there's a persistent failure mode that's not understood:
  no.

Determine that spare pool is sufficient, maintained, and will last to 2010:
  yes (7).

Determine that test facilities are sufficient and maintained(4):
  yes, at PREP.

Determine that expertise will be available and/or that system and procedures
  are documented: yes.
Software Documentation? Excellent.
Hardware Documentation? Excellent.

* ------------------------------------------------------------------------

Module: VTM  Quantity available: 65.  Quantity required 59.

Understand if specifications change now that 2010 is the expected lifetime
  due to increased radiation dose: n/a

Understand if specifications change due to performance expectations from
  other run2b upgrades: No.
```

Understand if specifications change due to changing accelerator conditions(3):
  No.

Understand if performance will meet the (new) specs in 2010:
  Yes.

Is there some way to help ensure or improve chances of successfully meeting
  specs in 2010 or whether significant improvement is possible: No.

Ask if there's a persistent failure mode that's not understood:
  no.

Determine that spare pool is sufficient, maintained, and will last to 2010:
  yes (7).

Determine that test facilities are sufficient and maintained(4):
  yes, at PREP.

Determine that expertise will be available and/or that system and procedures
  are documented: yes.
Software Documentation? n/a
Hardware Documentation? Good.

* ---

Module: FTM Quantity available: 65. Quantity required 58.

Understand if specifications change now that 2010 is the expected lifetime
  due to increased radiation dose: No noticable SEU rate.

Understand if specifications change due to performance expectations from
  other run2b upgrades: No.

Understand if specifications change due to changing accelerator conditions(3):
  No.

Understand if performance will meet the (new) specs in 2010:
  Yes.

Is there some way to help ensure or improve chances of successfully meeting
  specs in 2010 or whether significant improvement is possible: No.

Ask if there's a persistent failure mode that's not understood:
  receivers.

Determine that spare pool is sufficient, maintained, and will last to 2010:
  yes (7).

Determine that test facilities are sufficient and maintained(4):
  yes, at PREP.

Determine that expertise will be available and/or that system and procedures
  are documented: yes.
Software Documentation? n/a
Hardware Documentation? Needs update.

* ---

Module: DOIM receiver (RX). Quantity available: ~650. Quantity required (59*10)

Understand if specifications change now that 2010 is the expected lifetime
  due to increased radiation dose: expect little change.

Understand if specifications change due to performance expectations from
  other run2b upgrades: At limit, no significant speed improvement possible.

Understand if specifications change due to changing accelerator conditions(3):
  Not unless rate changes.

Understand if performance will meet the (new) specs in 2010:
  Expect it to, yes.

Is there some way to help ensure or improve chances of successfully meeting
  specs in 2010 or whether significant improvement is possible: No.

Ask if there's a persistent failure mode that's not understood:
  Yes/no (5).

Determine that spare pool is sufficient, maintained, and will last to 2010:
  yes, see David's chart in Figure 4. Failure rate <1/yr since 2003.

Determine that test facilities are sufficient and maintained(4):
  yes, at PREP.

Determine that expertise will be available and/or that system and procedures are document

Software Documentation? n/a
Hardware Documentation? (6).

* ---

Module: DOIM transmitter (TX) Quantity: All installed no changes possible.

Understand if specifications change now that 2010 is the expected lifetime
due to increased radiation dose: Changes prediced and operating parameter
changes should accomodate them.

Understand if specifications change due to performance expectations from
other run2b upgrades: At limit, no significant speed improvement possible.

Understand if specifications change due to changing accelerator conditions(3):
No.

Understand if performance will meet the (new) specs in 2010:
Yes, by definition.

Is there some way to help ensure or improve chances of successfully meeting
specs in 2010 or whether significant improvement is possible:
Check on annealing factors.

Ask if there's a persistent failure mode that's not understood:
No.

Determine that spare pool is sufficient, maintained, and will last to 2010:
n/a.

Determine that test facilities are sufficient and maintained(4):
n/a.

Determine that expertise will be available and/or that system and procedures
are documented: yes.
Software Documentation? n/a
Hardware Documentation? (6).
Specification documents for the above modules are available at
http://www-ese.fnal.gov/eseproj/index/svxii/svxii_family.htm

* ---

NOTES:

1-Measurements are currently being made such that single event upsets in
  the FIB requiring reload or reboot are counted but not logged.

2-FIB sequences are an issue. They are not documented well and some of
  the tools are very old.

3-In most cases the SVX chip readout speed sets the limit to readout. In
  some modules there are small speed increases possible but none is more
  than 20% or so. The named people can supply more details.

4-In some sense the existing test stands are use dependent. If they sit idle
  for a long time they tend to be cannibalized.

5-Some failure modes are well understood and some are still a mystery.

6-Existing documentation is dated, the best resource is corporate knowledge.

7-Primarily spares are modules, then some module components are stocked by
  equipment support at PREP.

* ---

Contacts from the spreadsheet:

Steve   "Steve Nahn, physicist, CDF Yale, nahn@fnal.gov"
Mark   "Mark Bowden, engineer, CD/CEPA/ESE, bowden@fnal.gov"
Ken   "Ken Treptow, Engineering Specialist, CD/CEPA/ESE, treptow@fnal.gov"
Stefano   "Stefano Rapisarda, engineer, CD/CEPA/ESE, rapisard@fnal.gov"
Tim   "Tim Kasza, equipment support, CD/CSS/ESD, kasza@fnal.gov"
Vince   "Vince Pavlicek, engineer, CD/CEPA/ESE, vince@fnal.gov"
David   "David Clark, physicist, CDF Brandeis, dkclark@brandeis.edu"

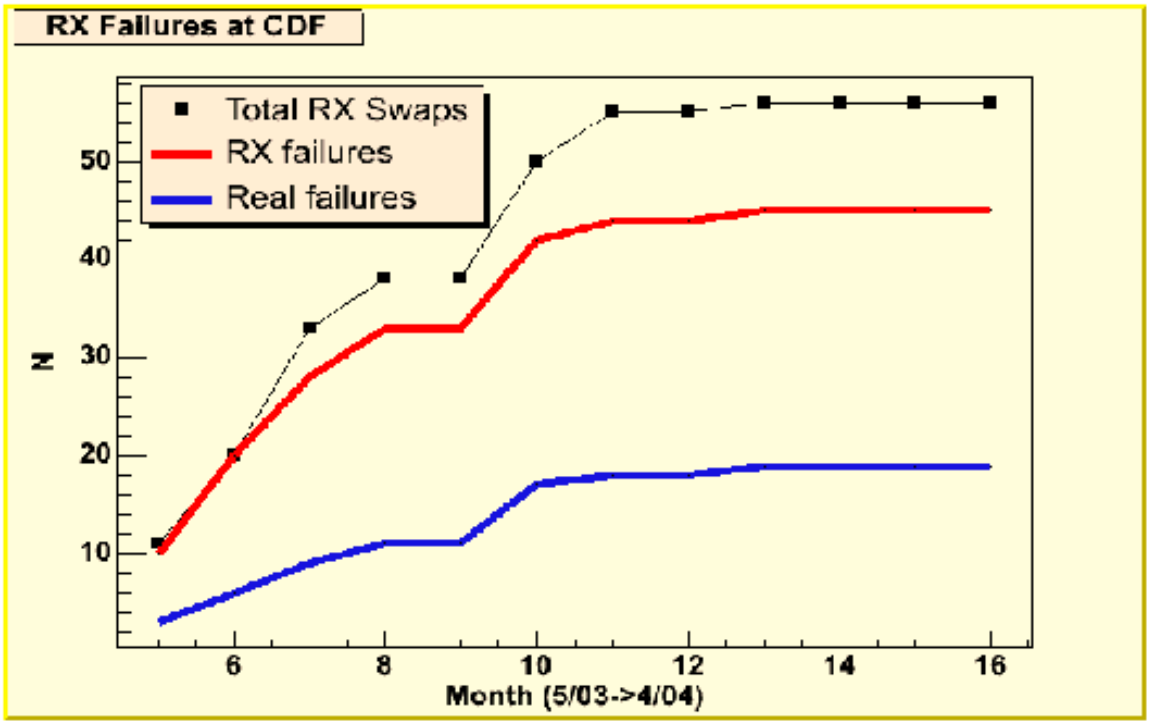

Figure 5: History of DOIM RX failures. Most failures are repaired at PREP and returned to the spare pool. The number of failures fell dramatically after gold-plating the connection pins in Oct-2003.

B SRC Vulnerability Study

```
* ========================================================================
* --- SRC Vulnerability Study
* --- original: 23-Apr-2004
* ---  updated: 21-Jun-2004
* --- D.Glenzinski, R.Wallny
* --- discussions with: L.Miller, G.Bolla, V.Pavlecek, S.Nahn, C.Hill, C.Gay
* ========================================================================
```

We examined the current SRC and evaluated its ability to reliably operate over the next 5 years. We'd like to note that the SRC, along w/ the interlock and cooling, are potential single-point failures for the silicon system as a whole. As such, it is imperative for this component to last throughout the whole of run2.

History:

The SRC has had no known hardware failures. There are 9 SRC boards total: 2 in operation in B0 first floor (taking data), 1 in B0 2nd floor (for testing), 2 in FCC DAQ2/3 teststands, 2 spares at FNAL, 1 spare at yale and 1 spare at harvard. There have been infrequent reasons to update the firmware. The most recent changes were in order to implement 2 SRC running (to circumvent L1 readout time of L00 (and ISL) which are not used in the trigger decision and so are now readout on a separate SRC.) However, several attempts were needed to iron out remaining issues of these firmware updates, some of which went badly in that they caused risk to the detector by causing high current states of the chips and/or unnecessary downtime.

It seems very unlikely that damaged SRC boards will limit the operational lifetime of the silicon system. However, since firmware changes have the possibility of damaging detector components, further changes should be made only when absolutely necessary. In those rare instances when a firmware change is deemed necessary, it should be very carefully considered and very thoroughly tested prior to implementation in the real system. Although no such changes are foreseen, it seems prudent to assume that some will be necessary prior to 2010.

Hardware Issues:

> the 4 spares at FNAL have not all had the complete set of ECOs implemented; we recommend that 5/6 be brought completely up-to-date

(both their hardware and firmware) and tested. the last should be kept as an emergency back-up (it still has the previous FPGA).

> only the EEPROMs occasionally have needed replacement; we should ensure we have a stack of spares

> the teststands are maintained and usable

Software Issues:

> the firmware can only be updated using a small number of PC running an old version of windows; the programming language is no longer supported; we should consider upgrading to a new language

> the firmware is not well documented; this should be remedied

> expertise resides in (mostly) one person, who will soon be moving on; must plan for this

> given the potential for damage, more realistic testing and a more thorough check-out procedure should be developed. the procedure should be very specific about how any upgraded firmware will be phased in (eg. first test on bench with hybrids, then on detector with guinea pig ladders etc.). this procedure should be written-up and formalized to include sign-offs from the CDF Ops Department (e.g. Rob Roser) and the Silicon SPLs. an example of such a procedure is the ‘‘Process Systems Change Request - procedure 110’’, which formalizes the testing and verifications which must be satisfied prior to introducing a change to the silicon interlock logic.

> due to "space" constraints, the aging firmware infrastructure, and other limitations inheirent in the board, the present SRC has little flexibility; it is difficult to know whether changing trigger or other operational conditions might warrant significant changes difficult to achieve with the present limitations.

Building a New SRC:

> with arrival of a new silicon system, a new SRC was proposed; since run2b has been cancelled, it’s not clear the upgraded SRC is necessary

> Advantages:

- could upgrade to improved hardware which may allow a larger
  L1 trigger rate (at present, it has not been demonstrated that
  the present SRC is the system limitation and, if so, that the
  proposed SRC would address the specific cause)

- could be designed to afford more flexiability to address
  future changes to trigger or other operational conditions

- could upgrade to modern (and more broadly supported) firmware
  and programming

- could develop new generation of expertise

  > Disadvantages:

- checkout and commissioning would incur some downtime and could
  potentially cause damage to the detector

- unclear to what extent the risk of detector damage can be mitigated
  with prior testing (ie. can teststand be made realistic enough?
  can specs be written explicitly enough? etc)

Findings:

Given that the present silicon DAQ+SRC meets the design specification
and has operated very reliably over the last three years, and
given that the specification is not expected to change - even with
Run˜IIB trigger and DAQ upgrades - we find no compelling reason to
advocate building a new SRC. Rather, we think it's more prudent to
spend the resources addressing the limitations of the present system.
In particular, we think the following should be pursued with the
highest priority

> Upgrade all but one of the spares to most recent ECO and firmware
  changes and develop a plan, in conjunction with the silicon SPLs
  and CDF Operations Dept, to thoroughly test these spares.

> Thoroughly document the firmware.

> Develop and document procedures for testing and introducing firmware
  changes into the B0 system. These procedures should be agreed upon

by the Silicon SPLs and the CDF Operations Deptartment and then formalized as a ‘‘Change Procedure’’.

> Ensure we have >1 PC running an OS that allows changes to firmware.

> Buy more EEPROMs if necessary.

Once a thorough set of firmware documentation is available, it would be prudent to explore (possibly using an engineering summer student) the possibility of migrating to a more modern firmware package. Vince Pavlicek has some specific ideas about what questions would have to be addressed in such a study.

One suggestion we have for helping develop a new generation of expertise is to: set-up tstand to develop 396ns (or 7bit digitization) sequencing; a new pdoc could be in charge of such a project as a means of developing expertise, firmware documentation, and making a more realistic test stand environment. This is quite an involved project and would require a dedicated effort from several people. However, it could prove extremely useful, especially in the event that we need to use 396 ns running in B0.

In the event that the specifications change or it is otherwised deemed necessary to build a replacement SRC, we would suggest the following:

> At a minimum, the new board should satisfy all the testing criteria required of firmware changes in the present system.

> At a minimum, a thorough list of Necessary and Forbidden sequences must be compiled; it must be demonstrated that the new board satisfies these requirements.

> Some thought should be given to the firmware and hardware choices with an eye towards maintenence through FY09.

> A detailed commissioning plan should be developed which should endeavor to minimize the following:

- silicon and cdf downtime; a parasitic commissioning plan would be ideal

- strain on silicon operations group

- risk of permanent detector damage

Some detailed email exchanges are included here.
* ==

From wallny@physics.ucla.edu Fri Apr 23 11:30:59 2004
Date: Thu, 22 Apr 2004 15:53:19 -0700 (PDT)
From: Rainer Wallny <wallny@physics.ucla.edu>
To: Douglas A. Glenzinski <douglasg@fnal.gov>
Subject: Re: SRC (fwd)

---------- Forwarded message ----------
Date: Sat, 14 Feb 2004 19:18:36 -0600 (CST)
From: Lester Miller <lmiller@harv11.fnal.gov>
To: Rainer Wallny <wallny@physics.ucla.edu>
Cc: adf@fnal.gov, rappocc@fnal.gov, Steve Nahn <nahn@fnal.gov>
Subject: Re: SRC

hi Rainer,

Some comments to your questions (others should also comment if needed)
>
> - how much headroom is left in this new chip for future improvement/
>   modification of the firmware ? We must have transgressed a boundary,
>   'how long' until we have to think switching again - if we can -
>   how many FGPA models are still pin compatible with the ones we use ?
>   will they be manufactured still in 5 years time or did we buy
>   enough for spare.
I don't know how much space is left but it should no longer be a limiting
factor for the SRC. We were at 90% but the new chip is a factor of two
larger so we probably are at 60% or so. While you can't go past 80% usage
to have routing issues, this still leaves some space. The real concern is
the other chips which were not upgraded especially the TSI emulator chip
which handles test stand modes and the inter-chip communication which
can't be addressed.
There is no longer a window of opportunity to replace these chips, and I
think we have no more. We bought literally the last 8 appropriate ones
available.
>
> - was sneezy not upgraded by accident (please don't) or is there a

>   technical reason ? In other words, how equal are the 9 SRC boards.
>   are they all on the same level ? if not, how many are interchangeable,
>   what are the quirks and idiosyncracies they have ?
We left one as failsafe backup without upgrade. The eight that are useable should all be interchangeable modulo firmware (and RSM chip). There are a couple of caveats. There are (I think) three modifications from production boards replacing some resistor arrays. I tried my best to get all on an equal footing but I think Steve still ran into one that was missing a mod. One board does not have a 53.103 MHz oscillator. (It has a cheaper 50MHz oscillator which cannot run in B0)
Note that there is an SRC at Harvard which is a complete unknown but should in theory be avialable if nine rather than eight SRCs makes some difference to planning
>
> 2) How many SRCs have been running in the full system ? I know of Dopey,
>   Sneezy and maybe a third whose name I have forgotton but most likely
>   lives in the test stand now.
This hasn't been kept track of.
>
>   once we will have overcome the latest firmware problem, would you
>   feel comfortable to have them rotate into the system as we are forced
>   to do power cycles for other reasons in order to prove that we indeed
>   have 'hot swappable' spares ? I am asking theoretically.
>
SRCs generally are being used by test stands. This may not be the case at this point as much as in the past. It may make sense for Sal to try to inventory each and make sure they all have the mods and the latest firmware. And also keep in a log which is where and whch one has the 50 MHz oscillator (and the older SRC FPGA) and what firmware version. Its been a perpetual source of confusion. Running them in B0 may be a good idea too but hard to find time.
> 3) How many legacy components, other than the FPGAs are on the board ?
>   do we have enough spare parts to repair a board ? has it ever happened
>   in the last 3 years that a board needed work other than on the FPGA ?
The only legacy components I can think of that may fail are used by CDF more generally, such as TAXI
receivers. But I think there's no way to buy any more of those. The good thing is that I've never seen a hardware failure in any of the SRCs.
The EEPROMS we use are in some sense a consumable and we should make sure we have enough to last x years. No reason not to buy the entire lot up front because they may get end-of-lifed although they are still available.
>
> 4) does programming the firmware require legacy hard- and software, ie.

>   are we running an outdated/unsupported version of a programming tool?
This is probably the most pressing concern for the board, the potential failure of the firmware programming chain. The firmware is progrrammed in a rather old version of Xilinx schematic entry, Foundation 1.2 I think, which is definitely legacy in that not only have several new version appeared, but Foundation as a software series has been superceeded and is no longer available. I don't know about backwards compatibility. This is one place we could throw some money, buy a license, and install the code on some more stable platform than a laptop running Windows 98. The key is that the software read and incorporate the file formats now used by the design which is both Xilinx Viewlogic and StateCAD diagrams, and can support these very old part designs (Xilinx XC3000,4000,4000E).
We can imagine buying an eprom programmer for the SRC if Yale gets tired of supporting this for us. Using ESE for this function was an unhappy state of affairs.
>
> 5) Who knows the firmware intimately enough that say they would be able
>   to program it from scratch or make modifications ? I know of Sal
>   and lester, maybe petar.
>   is the firmware documented in a way that it could be given to any
>   engineer who then could successfully implement it, or are we
>   relying on single individual's knowledge. I guess this point is
>   one of the most important.
The other option being discussed is rewriting from scratch in a new language (VHDL). This is an excellent way to migrate the responsibility for longer term maintenance. It carries substantial manpower cost and development/testing time. Aside from schedule risk there is some risk that a different language is not as efficient at translation/layout and will no longer fit into some of the more oversubscribed chips. With VHDL this is not trivial because how it is programmed can affect this.
But yes, we are relying on rapidly decaying expertise which will make new design changes meet a huge barrier to entry unless some rewriting along these lines is done. I don't know if it is justified in an approach involving freezing development. Risk in the form of some catastrophic firmware failure mode which would be unadressable in the current firmware framework is small (but nonzero).
The firmware is not documented. The act of documenting it would be as involved as rewriting it as far as I can tell which is why so little progress has been made in this area.

C Resonance GhostBuster Vulnerability Study

```
* ========================================================================
* --- Resonance GhostBuster Vulnerability Study
* --- original: 25-Jun-2004
* --- D.Glenzinski, R.Wallny, G.Bolla
* --- discussions with Taka Maruyama
* ========================================================================

 We examined the current Resonance GhostBuster board and evaluated its
 ability to reliably operate over the next 5 years.

 History:

 The Resonance GhostBuster has only been recently introduced into the
 silicon operations at CDF (May-2004).  It's comprised of a spare SVT
 ghostbuster board whose firmware has been written to identify trigger
 resonances which can cause wirebond failures.  In the event that such
 a resonance is detected, it throws an error state in the SRC.  It has,
 so far, worked without incident.

 Hardware Issues:

  > there is 1 spare SVT ghostbuster board;  there are 2 boards
    installed for SVT and another 1 board installed as our resonance
    detector. there have been no failures of the SVT boards since
    installation.

  > the resonance detector does not use all of the available channels,
    so that there is some "spare" capability even on the resonance
    board presently in use.

  > the teststands are maintained by UChicago; we should ensure this
    remains the case for our version of the ghostbuster board even
    after SVT upgrades


 Software Issues:

  > the firmware is broadly supported and there are numerous places
    which can burn it in

  > the firmware is not thoroughly documented; this should be remedied
```

> firmware expertise resides in one person; it's simple enough that, if documented, this should not be problematic - especially since changes are not, presently, foreseen

> need to ensure support, even after SVT upgrades

Findings:

Wirebond failures due to resonances _were_ a large source of permanent ladder damage. The frequency with which we will cross one of these resonances will increase as the trigger rate increases. As such it is extremely important that this Resonance GhostBuster board is maintained throughout the whole of RunII. We think the following steps ought to be taken to help ensure this:

> the firmware, although very simple, ought to be documented

> MOU responsibility ought to be taken for the maintenance of the board and firmware

> the system should be made to be self-monitoring or otherwise made to "fail safe"; presently, if the Resonance GhostBuster is not working (e.g. because the input connector is loose), the system still continues taking data without warning

D Junction Card Vulnerability Study

```
* ========================================================================
* --- Junction Card Vulnerability Study
* --- original: 25-Jun-2004
* --- D.Glenzinski, G.Bolla
* --- discussions with S.Worm
* ========================================================================
```

We examined the current Junction Cards and evaluated their ability to reliably operate over the next 5 years.

History:

The Junction Cards (JC) interface the digital, analog, HV, and timing signals from the CAEN crates to the tracking volume. They come in two pieces, an inner card and an outer card, both comprised of passive components only. The inner cards are very difficult to access and offer very limited possibility for repair. The outer cards can be accessed and even swapped (with some risk to surrounding JC) if necessary. The JC have been reliably working since installation. There has been one known failure of an outer card, which was successfully replaced.

It seems very unlikely that damaged JC will limit the operational lifetime of the silicon system. As a worst case scenario we consider the situation that a large fraction of the outer JC are damaged (e.g. from a power surge that goes unregulated through the CAENS).

Hardware Issues:

> there are 5 spare JC at FNAL; all have been tested and burned-in and are available as hot spares; there are parts for another 10-15 (except for 1 custom SAMTEC connector); a total of 114 JC are installed in CDF

> drawings are available to get more boards produced if necessary; the lead time is ~2 mos

> the board is stuffed with passive components; all are readily available; a custom 96 pin SAMTEC connector has a lead time of ~2 mos. all other parts are standard stock items

> once all components are in hand, an additional ~6wks would be necessary

to stuff, test, passivate and burn-in a full compliment of boards

Software Issues:

> none

Findings:

JC are not likely to limit the operational lifetime of the silicon system. In the event of a disasterous and systematic failure of a large fraction of the outer JC, all the drawings, hardware and testing procedures are available to replace the damaged cards on the timescale of 3-4 mos. Damaged inner JC cannot be replaced. Any systematic failure of inner JC needs to be taken very seriously and it's causes studied, understood and mitigated.

* ==========

E Cable Vulnerability Study

Silicon Detector Cables
Pat Lukens, May 2004

In principle, an inventory of every cable installed in CDF is available from the Cable Database. This can be reached from the Internet address http://131.225.234.72/Cable_Database_Default.htm. The investigation of the silicon detector cable infrastructure began with this database. Unfortunately, detailed examination of the database revealed that the information kept was either incomplete or clearly incorrect in many instances. The database is essentially useless, and cannot be considered to be an inventory of anything regarding the silicon detectors. A few examples of the problems are

> Optical cables listed as having LEMO connectors
> Cable counts that exceed expert counts by a factor of two
> Seventy one foot long cables that are listed as connecting the detector to the first floor counting room.
> Cables without wire or connector specifications
> Cables listed that were part of Run 1 and have long since been removed

The cable database appears to be incomplete, and perhaps corrupted. A strong recommendation should be to correct it, and provide a proper inventory of the CDF cable plant. While no investigation beyond the silicon system was done for this study, it is reasonable to assume that there are problems throughout and other systems will have incorrectly documented cables as well.

Several cables that are unique to the silicon system are listed in the table below, along with the appropriate quantities in use and the available spares. In general, testing of spare cables can be performed at the test stand that is maintained by the Computing Division. The silicon operations group also maintains a set of "load boxes" which can also be used in these tests.

In general these cables have been very reliable since the initial installation. Few or no failures have been seen since steady operations began. However, few spares of the DOIM and power cables exist, and obtaining more will be difficult and/or have a long lead time.

Recommendations:

> Update the cable database so that a useful inventory exists of each cable. Cable descriptions such as "3 Cond." should be replaced with

vendor part numbers.

> Cables that cannot be repaired should be identified and plans made for how we would react if they are damaged.

> Any change in installation plans that involves disconnection of the collision hall relay racks must consider the added risk to the cables. In particular, this applies to cables with low spares count.

Cable Type	Quantity in use	Spares Installed	Spares Elsewhere	Failures	Contact
HV Bias	144	0	3	0	Matt Herndon
SVX LV	84	0	2	0	Matt Herndon
ISL LV	30	0	1	0	Matt Herndon
Sense	114	0	3	0	Matt Herndon
FIB Timing	114	0	2	0	Matt Herndon
GLink 300'	58	4	2	$< 2\%$	Steve Nahn
GLink 80'	36	14	0	$< 2\%$	Steve Nahn
GLink 70'	42	0	2	$< 2\%$	Steve Nahn
DOIM	556	14	10	~ 5	Rong-Shyang Lu

Table 1: Summary of the number of silicon cables in use on the detector and their corresponding spares.

F Power Supply Vulnerability Study

```
* ========================================================================
* --- CAEN Power Supply Vulnerability Study
* --- original: 25-Jun-2004
* --- D.Glenzinski, G.Bolla
* --- discussions with M.Herndon
* ========================================================================
```

We examined the current CAEN power supplies and evaluated their ability to reliably operate over the next 5 years.

History:

The CAEN power supplies deliver the analog, digital, and bias voltages to the silicon detector. There are three "flavors" of CAENs, one each for the SVX, ISL, and L00. They also monitor the voltages and currents and interlock against some dangerous states. After some start-up pains and the replacement of some Micrel regulators (which were particularly prone to single-event upsets), the CAENs have been reliably operating. There have been no permanent failures of a CAEN power supply. There are lessor failures at the rate of about 2/year, which can be recovered by trained technicians. The CAEN company has promised to support these supplies for their entire operational lifetime. Also, in order to reduce the repair turn-around time, a technician at PREP (Hank Conner, hconner@fnal.gov) has been trained to perform the most common types of repair. We have not had to send a supply back to Italy in over two years.

The SVX and ISL supplies are capable of delivering up to 250 volts (+/-125 volts) at 5 mA on the bias lines. Since the coupling capacitors on the silicon sensors themselves are rated to 100 volts (and were burned-in at 90 volts), and the maximum current expected on the inner layers after 8 fb^-1 is only a few mA, the supplies should be readily capable of delivering bias voltages up to the capacitor rating for the whole of run2. The L00 supplies are capable of delivering 500 volts peak-to-peak on the bias lines and are also not expected to limit the operational lifetime.

There is a database which documents the history of each supply. It is available here:

http://www-cdfonline.fnal.gov/~reid/cgi-bin/psdb/DBmain.pl

PREP also keeps a database. There are 6 spare SVX supplies with 72

installed on the detector; 1 of these spares is used for a L00 wedge; there is also 1 proto-type SVX supply, which may be useful for benchtop studies. There are 3 spare ISL supplies with 30 installed on the detector. There is 1 spare L00 supply, with 11 installed on the detector; there is also 1 proto-type supply, which may be useful for benchtop studies. For bias voltages <250 volts, the SVX supplies can be used to supplement L00 spares.

It seems very unlikely that damaged CAENs will limit the operational lifetime of the silicon system. Similarly, the CAENs ought to be able to deliver the necessary bias voltage up to the coupling capacitor voltage ratings over the whole of run2 for all layers.

Hardware Issues:

- we should ensure that PREP agrees to maintain the technical repair expertise through the whole of run2

Software Issues:

- there are two software programs that have proven to be extremely useful in monitoring and controlling the power supplies: PS-GUI and IMON; it should be ensured that these are maintained throughout run2

The CAENs are not likely to limit the operational lifetime of the silicon. We should ensure that the MOU responsibilities are maintained both for the hardware maintenance, and the software monitoring tools (PS-GUI & IMON).

G Cooling Vulnerability Study

Silicon Cooling Vulnerability
08-July-2003

Rob Roser, Ken Schultz, Andy Hocker and Rich Stanek

We went over a list of areas that are potential problems for the cooling system in long term operation. This list might benefit from additional scrutiny and review by individuals close to the current operation of the system (such as Stefano Moccia, Bill Noe, and the Process System Operators).

There has been no attempt to quantify the cost of these recommendations or to rank order the priority. This can be done at a later date.

We identified the following areas of vulnerability:
> System Operation
> Corrosion/Erosion
> Sealant Degradation
> Radiation Damage
> Mechanical
> Technical Expertise

We'll separately discuss each of these below.

* ======================
* --- System Operation
* ======================

> Vacuum integrity of the system

The system was designed to run subatmospheric (2 psia). During the early operation of the system this was confirmed and there have been no real problems with continuing this operation as long as the vacuum pumps are in good shape. However, keeping the system vacuum tight takes vigilance and tight quality control.

Recommendation: Examine the data from system vacuum and pressure tests and determine if any negative trend is apparent. When a rate of rise is measured on the system, record it and compare to past performance. Try to include a quantification of the air bubbles in all of the system sight glasses. In a large system this can give valuable information.

> Response to failure scenario

  The silicon detector interlocks assume the availability of working
  instrumentation. Over time, there may be failures of temperature
  resistors or transducers that cannot be fixed.

Recommendation: Develop a plan to deal with broken
        instrumentation. Come to agreement as to how the interlocks will
        be modified when the input variable is no longer functioning.

> Pressure drop in the system

  Data is collected on pressure, pressure drop, temperature, flow and
  valve position for each 30 degree line.

Recommendation: Compare the data over time, assign someone to
        look for any trend that might indicate system degradation or
        clogging.

> Procedures

  The efficient operation and speedy recovery of the system from a
  failure requires that operators be familiar with the steps that should
  be taken.

Recommendation: Review procedures that are already written and
develop new procedures for step by step system recovery. Given
the current hours of operation, many of the possible failure modes
have already been encountered. Getting this experience translated
to a set of operating procedures is vital for long term system
stability

* ================================
* --- Corrosion of Al. and/or Be.
* ================================

> In the filtering section of the system (Alcove), specimens were placed
  in a sight glass (SVX has Be and Al, ISL just has Al).

Recommendation: When time permits, examine the specimens for

signs of corrosion. Also, check the filters for collected debris.
Try to quantify any observable changes.

> Periodically the system is shutdown and opened to either make
repairs or for access.

Recommendation: When an opportunity arises, take a sample of
fluid from each system and send it for analysis. Look for trace
amounts of Be or Al in solution or for any type of abnormal
suspended solids. Quantify and track results.

> The system has online conductivity measurement capability.
Recommendation: Examine the data for any trend in system
conductivity. This can be masked by periods where the system
is opened or by periodic changes in the resin bed.

* ========================
* --- Sealant Degradation
* ========================

> Epoxy/Sealants

There has been a long term study being run at Si-Det on the effect of
coolant on the integrity of the bulkhead joint. The 5:1 manifolds for
the SVX system initially had some problems with the glue/adhesive
used to seal the end plugs and the branches.

Recommendation: Continue this study and track periodic
examinations of the sample bulkhead and manifold. Record
leak test results and look for trends.

> Connectors/Joints

Initially there were several problems with the o-ring style connectors
used on the plastic tubing. In the end, this system was made to seal
leak tight and the performance over time (several
disconnection/reconnection cycles) has proven to be adequate.
However, these connectors require a "feel" to assure proper
engagement and quality control is essential.

Recommendation: For subsequent disconnect/reconnect cycles
continue to use "trained" individuals for this operation.

Develop a qualification exercise to expand the list of trained
personnel.

* ====================
* --- Radiation Damage
* ====================

> Radiation Damage to plastic components and epoxy

  Given that the expected lifetime of the detector was limited by
  radiation effects, the need to quantify the possible damage to the
  plastic tubing, connectors and epoxy was never questioned.

Recommendation: Study the possible long term radiation effects
for vulnerable materials within the range of CDF measured and
expected doses in the Central Detector. One concern may be the
softening of epoxy which is exposed to the combination of
deionized water and radiation. This is why the continuation of the
Si-Det bulkhead studies are important.

* ===============
* --- Mechanical
* ===============

> Spare Parts

  Although every effort was made to have a sufficient set of spare parts
  available for the system, it is unclear as to the present status.

Recommendation: Compile a spare parts inventory (online Excel
spreadsheet?) and assign responsibility so that it is kept up
to date as parts are used. Assure that all mechanically vulnerable
parts are covered, particularly pumps, valves and switches.

> Calibrations

  With the loss of some of the Lab's calibration capabilities particular
  attention should be paid to the transducers used to measure pressure
  and differential pressure.

Recommendation: Check the status of the spare transducers and
assure that CDF has at least one of each type and range that is
already calibrated and ready for installation.

> Periodic test of spare chiller

  The cooling system was designed with a redundant, online spare
  chiller system. This chiller has been used mostly as a backup for the
  ISL system (water only) but can be valved into the SVX system when
  needed. The key to using it on both systems is to assure that there is
  no cross-contamination.

Recommendation: In order to assure that the spare chiller is ready
when it is needed, it should be exercised "regularly". Put in
place a procedure that regularly tests the chiller as time permits.

> Verification of system interlocks and trips

  One of the problems with backup systems that are not "hot spares" is
  that one worries about assuring that the interlocks and trip points
  remain at the desired levels.

Recommendation: As part of the operating and maintenance
procedures prepare a way to test all of the interlocks on
each of the chillers to assure that they remain at the
desired set points.

* ==============
* --- Expertise
* ==============

> Expertise on mechanical system

  With the loss of Jim Ellermeier, much of the day to day knowledge
  and operating experience with the system is gone. As the system
  continues to run without incident the "collective memory" of the
  Operators on how to deal with an upset will diminish. Procedures
  offer one way to deal with a part of this issue but it is also important
  to have a resident expert who looks after the system.

Recommendation: Assure that the system is not "orphaned" by
assigning a senior-level mechanical person to be the resident
expert. This individual would need to be available at times of
system maintenance and recovery from upsets in order to gain the
most knowledge about system operation.

> Expertise on control system

  The same situation applies to the Texas Instrument Control System
  but it is even more extreme and possibly catastrophic. The
  programming of the TI system includes the interlocks and is integral
  to long term operation. Current system experts will "time out"
  without adequate overlap to new candidates. The fact that there is
  dual interlock control (TI and Quadlog) complicates the issue.

Recommendation: Develop a strategy for dealing with the
interlocks. One scenario would be to assure that present TI
system experts are replaced with new experts in plenty of time
to transfer information. Another strategy would be to convert
the entire interlock system to Quadlog and rely on current Lab
experts to maintain programming knowledge.

  NOTE: THESE CONCERNS ARE MORE EXPLICITELY ADDRESSED IN THE INTERLOCK
  VULNERABILITY STUDY.

* ===============
* --- Conclusion
* ===============

The CDF silicon cooling system has run for approximately 18 months with
very few major problems. Initial commissioning of the system discovered
several flaws in the original design and construction and all of these
problems were corrected with the goal of continuous, trouble-free, long term
operation.

This list of vulnerabilities was compiled with the idea of completeness. Not
all of these vulnerabilities are of the same level of concern and priority.

Given the operational history of the cooling system the major concerns would
be to:

1) Assure that technical expertise is maintained

2) Assure that spare parts are available

3) Assure that the spare chiller system stays a viable backup
   even after long periods of inactivity

H Interlock Vulnerability Study

Silicon Interlock Vulnerability Study

Doug Glenzinski, Rich Schmitt, Rich Stanek, Andy Hocker, and Rob Roser
April 7, 2004
Version 1.0

We examined the current silicon controls and interlock system and evaluated its ability to operate for the next 5 years and examined the risks.

```
* ================
* --- The System
* ================
```

The control and interlock system is built using Siemens QUADLOG safety rated PLC and peripheral modules as well as a Siemens 575 based PLC system. The QUADLOG system is programmed using function block diagrams while the 575 based system is programmed with ladder logic. Each PLC system has its own power supplies, chassis, backplane and readout modules. These systems read out a number of devices including pressure transducers, flow meters, and temperature sensors. Most of the system is readily accessible for access and repairs - the exception being the RTDs mounted on the silicon detector bulkheads.

```
* =============
* --- History
* =============
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The system has been very robust since its installation in 2000 at CDF. Since that time, there has been one documented failure of a Siemens 575 readout module. None of the RTDs (temperatures), pressure transducers, flow meters, or humidity sensors have failed to date. The software programs have been stable since 2001.

```
* =====================
* --- Hardware Issues
* =====================
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> Spares exist for all PLC modules with the exception of the 575 crate controller.

This spare may work but is currently not working in our test crate.

> Currently no working test stand

> Siemens long term support commitment to the 575 system is not known

> System is not well documented and existing documentation is not centralized in one location.

> Calibration of pressure transducers and differential pressure transducers should be updated. This was done prior to the system coming on line in 2000 but has not been done since.

* ====================
* --- Software Issues
* ====================

> Siemens 575 programming is done in ladder logic - it is not well documented

> Expertise in this programming language is limited; Andy Hocker on CDF and Dan Markley in the process systems group have the only local expertise

> QUADLOG programming with its function block diagrams is self-documenting. A number of process systems engineers at the lab are comfortable programming in this language

* ============================
* --- Modernizing the system
* ============================

With the expected arrival of a new silicon detector, new controls and interlock hardware were purchased. With the cancellation of the run2b silicon project, the case for swapping the interlock/controls is less clear.

The new system is an APACS/QUADLOG that's safety rated to handle interlocks. APACS would handle the controls logic. The advantages over the present system are:

> Control and interlock would be explicitly separate. That is not the case at the moment.

> There are a number of process systems engineers at the lab that are

familiar with the QUADLOG programming, so there'd be a wider redundancy of programming expertise.

> Spares already on hand - these systems are currently in use for CDF's remaining process systems.

The disadvantages are

> Checkout of a new controls and interlocks hardware is painful - there is some risk that the detector will be damaged during checkout and commissioning and/or due to a mistake or fault in the new system

> While rewiring is being done, the silicon cooling would have to remain off. Initial estimates of 4-8 weeks (although Rob thinks that with careful planning and parallel operations this may be reduced to ~2wks)

> Reprogramming requires substantial effort and extensive checkout. Checkout procedure should be thought about and documented a priori.

Some of the risk and much of the work can be reduced if there's a board which allows APACS/QUADLOG to communicate directly with the SIEMENS 575 I/O modules. Rich Schmitt is trying to see if such a board exists for our flavor of the SIEMENS crate. If this is the case, then NO re-wiring would be necessary - only the software would have to be re-written and checked-out. The silicon would still have to be off for this checkout.

```
* =================
* --- To Do List:
* =================
```

Rochester

> Setup spare test crate at B0 to be used as a test stand
> Repair 575 module/test crate so that we have a working spare (Find out why it failed)
> Mock up a portion of the actual system and use that to train Dan Markley on our systems so that there exists a backup software expert
> Update the interlock code so that power is dropped to the backplane when requested - in other words implementing a workaround to the 5v enable firmware bug.

Schmitt

> Contact Siemens and understand how long the 575 system will be supported

> Determine whether there is a module that allows one to talk from APACS to the 575 like there does for the 505 module
> Estimate the amount of time it would take to rewrite existing software in 4-mation

Roser
> Assemble book with all relevant interlock documentation

New Post Doc
> Read and document the current Siemens ladder logic programs

Group
> Decide whether to embark on a new interlocks project based on the above information. Some "decision deadline" should be determined in discussions with Operations, Silicon SPLs and the relevant experts.

Some additional issues include:

1) Training: you mentioned getting Markley up to speed on this system, but I also think that there needs to be a plan for succession of the Rochester Expert (including time to train) and a plan to train some of the operators on how to respond or solve simple (most probable) failures/interlock issues. For the cooling system there are really 3 levels of interlocks (Quadlog, TI, and internal chiller interlocks). Keeping people familiar with the response to very rare failures is always a challenge.

2) Documentation : Make sure the list of spares is up to date (both for mechanical parts and PLC cards). Also decide on the need to be able to do calibrations when needed (Is PAB still an option?)

3) PC failure : The issue of the critical nature of the single PC that is the interface from the PLC to the iFix displays needs to be considered. Is there a way to parallel signals?

4) Update any old wiring diagrams (not a big problem).

I Radiation Safety Vulnerability Study

Radiation Safety of the CDF RunII Silicon Detectors

Jeff Spalding
June 2004
version 2

Three areas were considered.

1) RADMON : Protection from a [relatively] slow radiation incident, and prevention from repeating such incidents.

2) Fast Beam Accidents : We have little protection. How can we improve the protection we have and reduce the number of such incidents?

3) TEVMON : Monitoring store conditions and alarming if the store is abnormal. Beam in the abort gap produces a particularly serious alarm.

* ================
* --- RADMON
* ================

Background:

RADMON alarms on a high integrated dose to the silicon and aborts the Tevatron automatically on a high dose rate. No single accident will account for a large fraction of the total life expectancy of >1 Mrad in fact the Tevatron will quench and abort well below 1 krad. The emphasis is to limit the number of such accidents rather than to prevent damage from any single accident. There are procedural aspects to RADMON, unlike an interlock system.

RADMON has been in use since 1992. See CDF note 5414 for a description of RADMON at the start of Run II.

Radmon uses standard loss monitors for radiation detection (as used throughout the Accelerator Division), but custom CAMAC modules for reading out and applying thresholds. These modules are supported by Accelerator Division (AD). The electronics have been alive in a warm crate for 12 years of which it was active for 4-5 years. No hardware changes were made for Run II, but thresholds were redefined. D0 made an identical system in 2000 for Run II.

RADMON generates an integrated dose alarm, and aborts the Tevatron on a high dose rate. Both situations require a response form the SCICO and RADCO, as described in CDFII Proc 106. (Procedures are summarized in the online help for the monitoring ACE, but I can't find them on the SCICO page. The procedures are nicely summarized at: www-cdfonline.fnal.gov/mcs/radmon/response.html.)

AD is considering developing a new readout system for the loss monitors in the Tevatron, to be completed by the end of 2005. The new system could probably provide the functionality needed by RADMON.

RADMON has worked well, with no serious failures. And if there were a failure, it is highly unlikely that serious damage to the detector would result. However, there are some concerns for the long-term, including long-term maintenance of the CAMAC system and the procedural nature of operations, especially as personnel change.

Recommendations:

1) We need a commitment from AD to maintain the CAMC modules through 2010. The need and goals for RADMON are unchanged. Thresholds will likely remain unchanged, but may need to be adjusted. This requires burning new tables into EPROMs. The EPROM chips, and the burn-station are old.

2) Simplify procedures, formalize RADCO training, and add to Ops Manager training. Consider (again) a DC voltage/current for self-monitoring and alarming in ACNET. No failure mode has been uncovered, but there is a risk of both operational confusion (likely) and operational failure (less likely) due to the dependence on procedures. These risks can be mitigated by simplifying and formalizing the procedures.

   * The system fires rarely enough that the CDF and MCR crews are not familiar with it. Procedure 106 should be both simplified and expanded. The threshold table in use is already a lot simpler than the one described in the procedure. The procedure should include information on the ACNET pages and FIFO logging.

   * Replace the threshold page with a crash button for manual abort. This should be the same for D0, so needs to be coordinated with D0 and MCR.

   * The BLMs must often be removed and replaced for accesses. After each occurrence, and after each power outage, the RADCO must follow a test procedure to verify the system integrity. This should be formalized in

the RADCO and Ops Manager training. The Ops Manager should confirm that the RADCO has performed the verification.

3) A commitment is needed from AD for the support of the CAMAC modules through 2010, including burning the EPROMs.

4) In addition CDF should consider the proposed VME based system for Tevatron loss monitors and ensure that it can provide equivalent functionality.

The CAMAC modules consist of a coupled pair of cards (numbers 335 and 336).
335-336 pairs:
CDF use=2, spare=1
D0 use=4, spare=?
The system is vulnerable to a catastrophic incident, due to a lack of spares. A decision to continue to maintain the CAMAC system, or to switch to the new system (in early 2006) would depend on operational experience and an assessment of the work and risk associated with the new system.

* ==============================
* --- Fast Beam Accidents (FBA)
* ==============================

Background:

An unexpected SVX failure mode (called AVDD2 failure) occurs with some probability for a specific class of beam accidents. The failure results in the fatal loss of function from part of a ladder. The present (limited) understanding is that the damage is caused by a very rapid radiation incident. The dose can be very low (a few rads) but the time scale must be very short (likely 100s nsec). It is likely that the initial damage is related to a current surge into the front-ends of the SVX3 chips. The actual failure mechanism is not yet understood and may include damage internal to the chip or the failure of components or connections on the hybrid. There is some evidence that thermal stress may exacerbate an existing intermittent failure.

Recommendations:

Three mitigations are disscussed below:
1) reduce exposure to fast beam accidents
2) reduce the number of power and thermal cycles to the detector
3) care and feeding of damaged ladders
For the silicon detector to survive through 2010 it is essential that these

efforts be pursued aggressively.

1) Reducing exposure to fast beam accidents
If the silicon is to survive through 2010, additional emphasis is required here. The only known accelerator action which can result in a sufficiently rapid delivery of dose at CDF is a kicker fire occurring while beam is passing through the kicker - a misfire.

CDF should work with the AD abort task force to ensure that

A) the probability for a kicker misfire is minimized. there are several scenarios here:

> the kickers fire normally but there is out of time beam in the abort gap

mitigated with the TEL and by CDF using TEVMON to monitor beam in the abort gap

> kickers are mis-timed and fire outside of the abort gap

mitigated with procedures for timing in the kickers (not yet formalized?) and by the addition of hardware to safely accommodate a loss of timing information (done) the loss of AC power (planned)

> one kicker spontaneously pre-fires - no abort is pulled

mitigated via kicker conditioning procedures (is this documented?). it may be possible to redesign the abort region to reduce the number of kickers required (and therefore the misfires) by a factor 2.

B) the probability for any dose at CDF is reduced when there is a misfire

> collimators at A11 and A48 are intended to minimize the dose at CDF by shadowing B0 from the kickers; clearly this shadowing is imperfect; are the collimators optimally positioned?

Kicker pre-fires cannot be prevented. But with the cancellation of the Run IIb upgrade it has become more critical to reduce the pre-fire rate (for example a factor two would make a big difference) and to improve collimator protection if possible.

2) Reduce the number of power and thermal cycles to the detector
This is achieved via the present procedures for operating the silicon detector and through the vigilance of the SPLs and CDF Operations Managers. The only action here is to emphasize the obvious importance of information hand-over when the personnel in these positions change.

3) Care and feeding of damaged ladders
There should be further study of the mechanism of AVDD2 failure. Early analysis suggested either wire-bond failure, the failure of a silver epoxy joint, or failure of circuitry inside the chip, but extensive radiation exposure testing and bench testing failed to reproduce the failure. While it is highly unlikely that a fix is possible, an understanding of the mechanism may lead to improved mitigation of further damage.

There have been cases where AVDD2 failures were recovered, at least temporarily. Such cases should be documented so that similar approaches can be tried in the future.

* ============
* --- TEVMON
* ============

Background:

TEVMON is a monitoring application running in the CDF control room. It uses input from the Beam Shower Counters, Rick's Counters and ACNET to monitor loss conditions in the Tevatron. The devices monitored are listed at
http://www-cdfonline.fnal.gov/online/tev.html
TEVMON really has two functions. The first is to monitor losses or other general conditions in the store - principally LOSTP and LOSTPB and the RMS variation in these. An alarm informs the shift crew that losses are high or unstable and they should take some action. The second is to alarm on high losses in the abort gap which can lead to an FBA on a perfectly normal abort. The current procedures for this alarm are at
http://www-cdfonline.fnal.gov/opshelp/abort_gap_policy.html

TEVMON works well. Maybe the "this is a lossy store" and the "danger! beam in the abort gap" aspects should be called-out separately. The former is probably an operational issue for the whole detector before it's a safety issue for the silicon, while the latter is certainly a safety issue for the silicon detector (Rainer may disagree - there is ongoing discussion about the danger posed by high losses and appropriate thresholds.)

In addition to monitoring abort gap losses, TEVMON checks that the TEL is on. Without the TEL the abort gap danger level will inevitably be reached in the near future.

The counters at CDF measure locally lost beam halo during the abort gap. This is an indirect measure of the total amount of beam in the gap. While it may give an appropriate relative measure of the total beam in the abort gap during long-term steady operation, scraping with collimators might significantly and immediately reduce this halo component more than the central component - giving an optimistic impression of its effectiveness. Over tens of minutes the measure will return to the steady state.

AD expects to have a direct measure of the amount of beam in the abort gap using the synch-light detector, by sometime in June-2004.

Recommendations:

1) Improve TEVMON documentation.
   The Tevmon webpage/document describes what Tevmon does and what is displayed. There should be more information or a companion webpage or document which lists the Tevatron features that the silicon system relies on and why - TEL, collimator positions, RF voltage abort threshold, the abort logic itself and the kicker timing.

2) Rick's counters should be set up and maintained in a robust, self-testing manner.

3) The synch-light measurement should be added to TEVMON (in addition to Rick's counters). This might become the primary measure for alarms, with Rick's counters becoming additional information. Certainly much might be learned by comparing the two.

4) perhaps the beam position at A0 should be monitored?

5) perhaps the LostP and LostPbar Thresholds should be Revisited. these thresholds are difficult because it's not entirely clear how to set them or otherwise establish in an a priori manner what's safe. so far they've been set by "historically" considering what loss rates look like for good runs.

6) Optimize collimator settings.
   Once the synch-light abort measurement is available, a dedicated

proton-only study period should be used to measure RADMON dose versus abort gap content for an abort. This should be done initially for the standard collimator positions at A11 and A48 (measured relative to beam position I think). (Standard procedures for where to set the collimators should be defined before this study.)

Once this data is digested, a second scan with collimators moved out a little will provide very useful information on our sensitivity to their position - relevant both here and for the kicker misfire discussion above.

J Knobs We Have to Change Signal-to-Noise Ratio

Knobs we have to recover S/N in the future.

Gino Bolla
May 20, 2004
Version 1.0

The current silicon system has been examined and possible ways to recover performance after degradation induced by radiation damage are described.

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* ==================================
* Signal-to-noise ratio degradation
* ==================================
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The signal-to-noise ratio of the silicon ladders in the CDF system will be degraded by radiation damage during run2. The main contributions to the degradation are:

1. Increase in the shot noise due to the increased leakage current on the silicon sensors

2. Decrease of Charge Collection Efficiency (CCE) due to trapping in the silicon bulk and due to the increased charge collection time.

3. Decrease of single hit resolution due to the decrease of the inter-strip resistance

4. Decrease of the chip performance

These effects are inevitable but there are a few parameters that can be changed in the CDF silicon system which might (partially) compensate for these degradations. These parameters are:

A. The silicon sensor temperature
B. The integration time of the SVX3d chips
C. The integrator NMOS bias current and Bandwidth settings on the SVX3d chips

In general it is recommended to implement or improve the monitoring tools to be able to monitor the following:

> Signal, Noise and Signal-to-noise ratio on a ladder-by-ladder basis,

for phi and stereo sides separately, as a function of integrated luminosity with a granularity of approximately 200 pb-1.

> Single hit resolution on a layer-by-layer basis, for phi and stereo sides separately, as a function of integrated luminosity with a granularity of approximately 200 pb-1.

Each of the compensating parameters are discussed briefly below.

* ====================================
* --- The silicon sensor temperature
* ====================================
When the single strip leakage current on the silicon sensor reaches the uA range the consequent shot noise becomes comparable with the noise due to the capacitive load. The two components add in quadrature to each other. The shot noise is proportional to the square root of the leakage current with constants that are dependent on the rise time and integration time of the FE amplifiers. A comprehensive description of the expected noise behavior can be found in CDF note 3278. With single strip leakage current in the few uA range the shot noise will be dominating. A decrease in temperature of 7-8 deg-C would imply a reduction by a factor of 2 in the leakage current and a consequent 40 % reduction on the shot noise component. The CDF silicon cooling system is now being used with a coolant temperature of -6 deg-C. The design goal was -10 deg-C and there is probably headroom for even lower temperatures.

Recommendations:

> Understand the lowest possible chiller temperature of the Silicon cooling system.

> When a signal-to-noise ratio degradation of 10% or more is detected a noise versus temperature scan should be performed. A 10 deg-C variation of the chiller temperature from the nominal upward is considered enough to provide the information necessary to extrapolate the impact of a lower chiller temperature in the shot noise component. The temperature range being scanned should be minimized in order to avoid thermally related failures

* ====================================
* Integration time of the SVX3d chips
* ====================================

The bunch crossing spacing at CDF is 396 nsec. The Tevatron upgrade to 132

nsec bunch spacing has been canceled. The CDF silicon system FECLK cycle is still 132 nsec. There are potential advantages and disadvantages on changing the silicon integration time from 132 to 396 nsec. By comparing Figures 6 and 7 it is clear that the charge sharing is worse for the 132 ns FECLK. This additional charge sharing affects the distribution of the collected charge and consequently the single hit resolution . This effect is reduced if the integration time is increased to 380 nsec.

Potential advantages:

> Improved online efficiency due to the larger charge collected in the central strip(s) of the clusters

> Improved single hit resolution by potentially compensate for the widening of the cluster size due to the inter-strip resistance degradation.

> Decrease on the noise component associated with the capacitive load (by choosing the highest Bandwidth setting that is compatible with the 396 nsec mode)

Potential disadvantages:

> Increase on the number of noisy channels and their noise level on the so called (micron) grassy ladders. These ladders dominate the SVX readout time (and, therefor, can affect L1 trigger rates and SVT timing).

Recommendations:

The CDF silicon system has never been operated with a 396 nsec FECLK cycle. The investments on the DAQ in order to cope with the change are yet unknown so it is recommended to evaluate the impact of the longer integration time on spare ladders post-exposure to irradiation.

> Irradiate a L0 spare ladder with a variable fluence along the Z direction with a maximum fluence consistent with the expected maximum goals for the Tevatron delivered luminosity profile.

> Test the charge collection properties in 132 and 396 nsec modes with the existing svxdaq and 1064 nm laser.

> Investigate the compatibility of the present DAQ with the longer FECLK cycle.

* ================================
* ISEL and BW SVX3d chip settings

* ================================

A very detailed study of the effects of these parameters on the signal-to-noise ratio for L00 is documented in CDF note 5262. After irradiation the signal-to-noise ratio was increased by running the SVX3d chips with increased integrator current. In order to take full advantage of this feature the L00 hybrids have been assembled with a smaller resistor for the ISET (9K? with respect to the 14 K? of SVX II and ISL). Up to a 25% increase in the signal-to-noise ratio post irradiation was measured for the irradiated L00 modules. A similar approach should be applied to the innermost layers of SVX II by measuring the signal-to-noise ratio with the highest integrator current. The current of the integrator is set by 4 of the remotely programmable ISEL bits in the chip bit-stream. As a consequence tests can be carried out on single ladders before being applied to the whole system.

Potential advantages:

> Improved signal-to-noise ratio after sizable radiation damage

> Slower rise time and potential improvement in the performance in 396 nsec mode

Potential disadvantages:

> Increase in the current consumption on the analog part of the SVX3d chip with the potential of increasing the rate of AVDD2 failures.

Recommendations:

> Chose a subset of ladders in the innermost SVX II layer and measure the signal-to-noise ratio for the default and the maximum integrator current settings.

> Depending on the results expand the changes to the other ladders of the same layer.

This effect is documented on Igor Volobouev's presentation at DPF2002 that is available from the CDF silicon web pages.

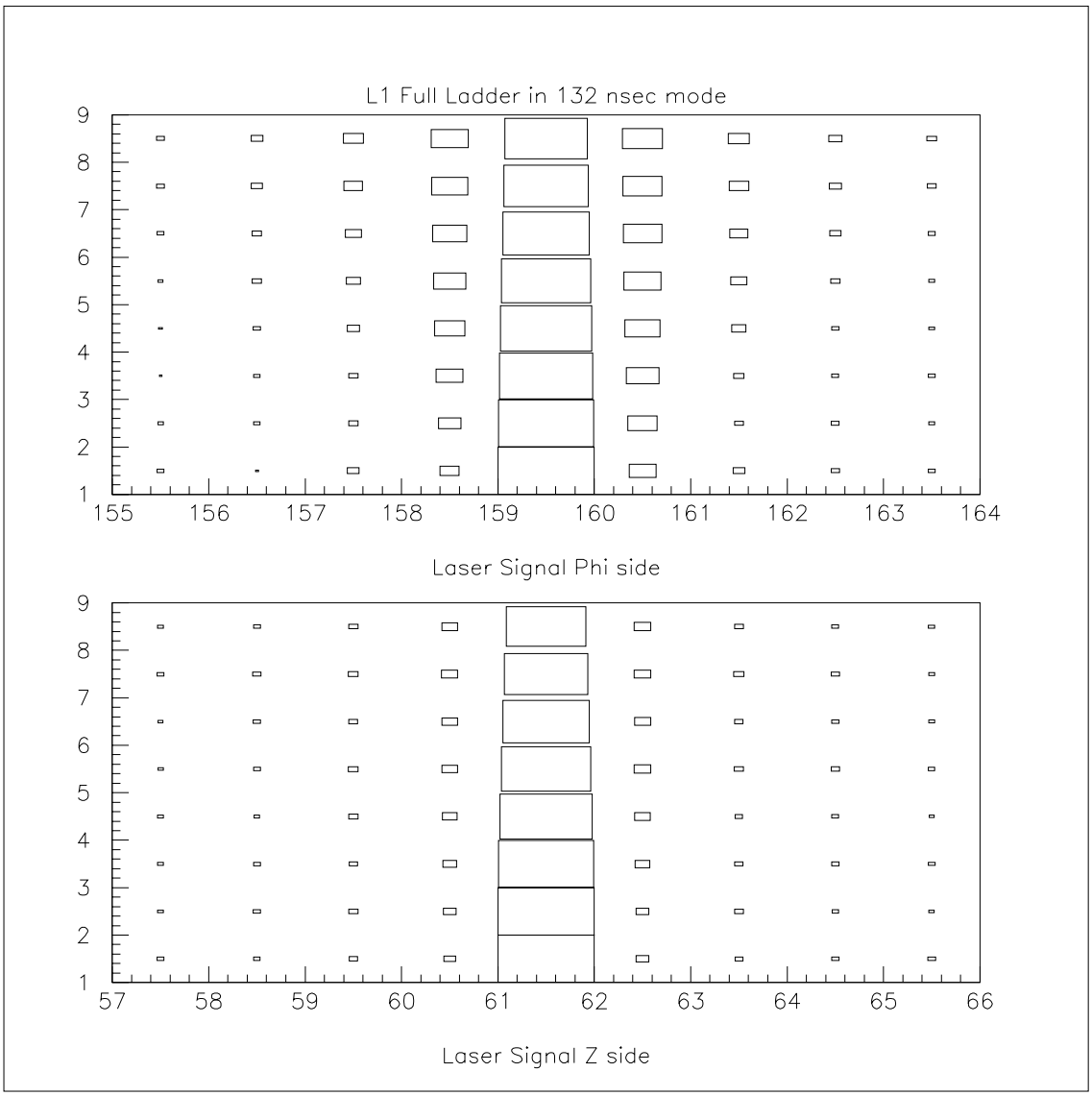

Figure 6: Laser induced signal on a layer 1 SVX II ladder. The X axis is the channel number while the Y axis is the BW settings. These plots correspond a 140 nsec FECLK cycle (120 nsec integration time) and should be compared to the corresponding plots made with a 400 nsec FECLK as shown in Fig 7.

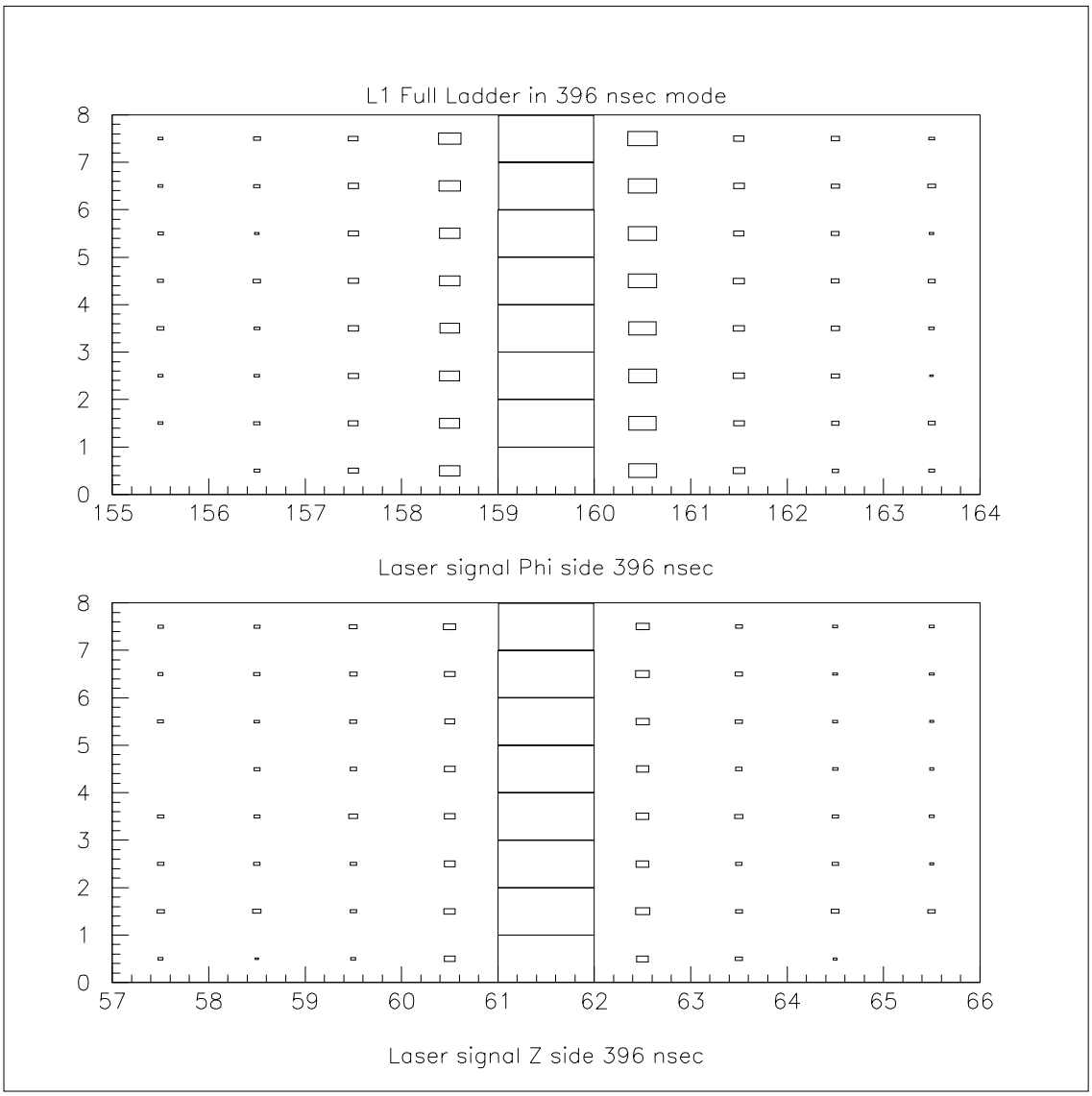

Figure 7: Laser induced signal on a layer 1 SVX II ladder. The X axis is the channel number while the Y axis is the BW settings. These plots correspond a 400 nsec FECLK cycle (380 nsec integration time) and should be compared to the corresponding plots made with a 140 nsec FECLK as shown in Fig 6.